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Spiking and Bursting Firing Patterns of a Compact VLSI Cortical Neuron Circuit

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***Abstract*—The paper presents a silicon neuron circuit that mimics the behaviour of known classes of biological neurons. The circuit has been designed in a 0.35µm CMOS technology. The firing patterns of basic cell classes: *regular spiking* (RS), *fast spiking* (FS), *chattering* (CH) and *intrinsic bursting* (IB) are obtained with a simple adjustment of two biasing voltages. The simulations reveal the potential of the circuit to provide a wide variety of cell behaviours with required accommodation and firing frequency of a given cell type. The neuron consumes only 14 MOSFETs enabling the integration of many neurons in a small silicon area. Hence, the circuit provides a foundation for designing massively parallel analogue neuromorphic networks that closely resemble the circuits of the cortex.**

I. Introduction

BIOLOGICAL systems are capable of handling high computational throughput of sensory perceptions, cognitive processes, decision making and motor control with low energy consumption. The psychophysical signal processing takes place in networks of cortical microcircuits and their main constituents are neurons and synapses. In the hope of emulating some of the brain's intelligent processing, mimicking its operation in silicon is a subject of ongoing research interest [1-7].

An important consideration when designing large-scale massively-parallel VLSI models of neural processing, is the silicon area consumed by the circuitry. The Integrate and Fire (I&F) neuron model is widely used due to its simplicity - typically used I&F neuron cells consume approximately 20 transistors to implement low power adaptive neuron circuitry [8] [9]. However, I&F neurons exhibit simple firing behavior only - this might not be adequate for the development of VLSI circuitry which would be capable of imitating the processing of human cortex, which is made of a large number of more complex non-linear oscillatory neurons exhibiting a variety of inherent firing patterns. Circuits implementing conductance-based neuron models (Hodgkin-Huxley type) have been reported in the literature [10] [11], however, these circuits consume a large number of transistors. The circuit implementations of oscillatory neuron models such as the FitzHugh-Nagumo [12], Morris-Lecar [13], Resonate-and-Fire [14], Hindmarsh-Rose [15] or Hardware Oregonator [16] have consumed around 20 transistors. However, all these models do not reproduce accurate shapes of the spikes generated by biological neurons and are not capable of producing different types of cortical spiking and bursting behaviours in a single circuit with tunable parameters.

In this paper we present a simple CMOS circuit model that exploits underlying nonlinear characteristics of MOS transistors to implement the neuron using only 14 transistors. The spiking shape given by the circuit resembles that of real neurons. The circuit is capable of producing linear and non-linear responses, with complex spiking patterns such as regular spiking, fast spiking, low threshold spiking, intrinsic bursting and chattering.

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II. Firing Patterns of Cortical Neurons

Biological neurons can be classified into different types, depending on their electrophysiological response to a specific stimulus [17-19]. A neuron responds to a step injection of *supra-threshold current* (post-synaptic input current that causes *action potentials*) producing either spiking or bursting firing behavior. Note that the characteristic firing patterns discussed further in this section can be seen in simulation results shown in Fig. 7 and Fig. 12. For comparison, the spike waveforms obtained via electrophysiological recordings can be seen in [17-19].

The spiking neurons are of two types, *regular spiking* (RS) and *fast spiking* (FS) [17]. The RS cells fire repetitively with a progressive decrease in firing frequency when a supra-threshold input current is sustained [18]. The FS cells fire repetitively at high frequency with little or negligible *accommodation* to a sustained supra-threshold current. The accommodation (also known as *adaptation*) is the progressive decrease in firing frequency despite the maintained depolarization. The action potentials of FS cells exhibit faster rise rate, fall rate and distinct fast *afterhyperpolarization* (AHP) [19]. Neurons with FS behavior commonly found in the cortex are for example neocortical s*mall basket cells*, *nest bouquet cells*, *bitufted cells* and *large basket cells* [18]. The RS cells can be further subdivided into two subtypes depending on their accommodating property inherent in the repetitive firing pattern; i.e. the weakly accommodating cells are classified as RS1 and strongly accommodating cells are called RS2 type[18]. Examples of morphological cells that behave as RS1 type are neocortical layer II-VI *pyramidal cells*. The RS2 type cells are neocortical layer IV-VI *pyramidal cells* and s*piny stellate cells* [19].

The basic bursting cell types are *chattering* (CH) and *intrinsic bursting* (IB) [17]. The CH neurons usually display repetitive long clusters of spikes to a sustained supra-threshold current injection. IB neurons discharge with a cluster of three to five spikes (referred to as a burst), followed by an AHP, and then by either single spikes or burst at more or less regular intervals [18]. These types are observed in sub populations of *bitufted cells*, *bipolar cells* and *martinotti cells* in the neocortex [19].

III. PROPOSED CIRCUIT

The proposed circuit is presented in Fig. 1. The implemented model consists of two state variables represented by voltages across capacitors C_V and C_U, One corresponds to the "membrane potential" (V) and other corresponds to the "slow variable" (U). The evolution of these two state variables, together with a resetting mechanism, resulted in a variety of bursting and spiking neuron behaviours, controlled by the voltages at nodes labelled c and d. This is similar to the model proposed by Izhikevich [20]. Based on the first order circuit analysis the following equations can be obtained:

$$\dot{V} = \begin{cases} l_1V^2 - l_2V - l_3U^2 + l_4U + l_5 & \text{when } V \geq U - V_T; \\ m_1V^2 - m_2V - m_3UV + m_4 & \text{otherwise} \end{cases} \quad (1)$$

$$\dot{U} = k_1V^2 - k_2V - k_3U^2 + k_4U + k_5 \quad (2)$$

$$\text{If } V > V_{th} \text{ then } \begin{cases} V \leftarrow C \\ U \leftarrow U + D \end{cases} \quad (3)$$

where, k_i, l_i, m_i, V_T, V_{th}, C and D are constants depending on transistor parameters (e.g. W/L ratio) and regions of operation, bias voltages and synaptic input current.

The circuit comprises three functional blocks, the membrane potential circuit (transistors M1-M5), the slow variable circuit (transistors M1, M2 and M6-M8) and the comparator circuit (M9-M14) as shown in the Fig. 2 (a), (b) and (c) respectively.

The membrane potential circuit is shown in the Fig. 2(a). The post-synaptic input current, (excitatory or inhibitory), plus the current provided by M3 (which is a function of the membrane potential and provides the positive feedback that generates the spiking), minus the leakage current generated by M4, are integrated on the capacitor C_v to provide the membrane potential V.

Once the membrane potential reaches its threshold voltage, V_{th}, the comparator generates a pulse V_A, as shown in Fig. 3(b) that resets the membrane potential through the transistor M5 to a value set by the voltage V_c.

The slow variable circuit is shown in Fig. 2(b). The current provided by M7 (which is a function of the membrane potential), minus the current drawn by M6 (which is a function of the slow variable potential) are integrated on the capacitor C_u to provide the slow-variable potential U. When the membrane potential reaches the threshold value, the comparator generates a pulse, V_B

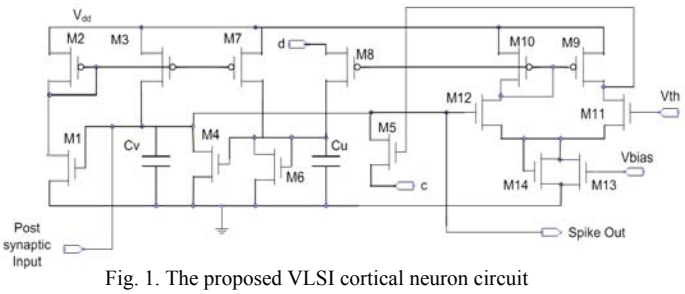


Fig. 1. The proposed VLSI cortical neuron circuit

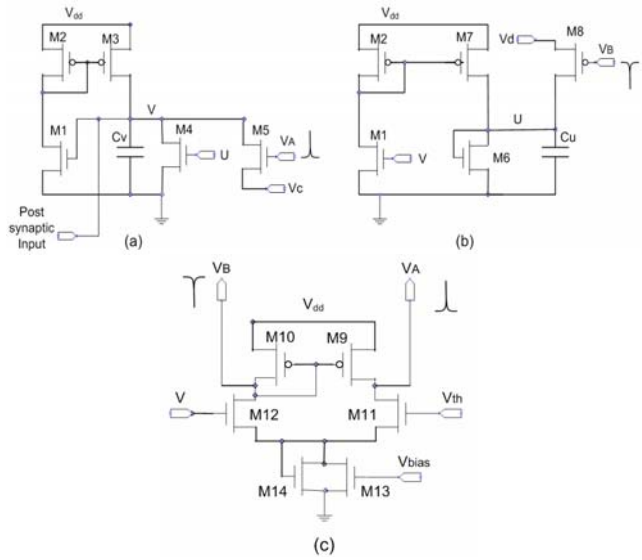


Fig. 2. Sub-circuits of the proposed VLSI cortical neuron. (a) Membrane potential circuit. (b) Slow variable circuit (c) Comparator circuit.

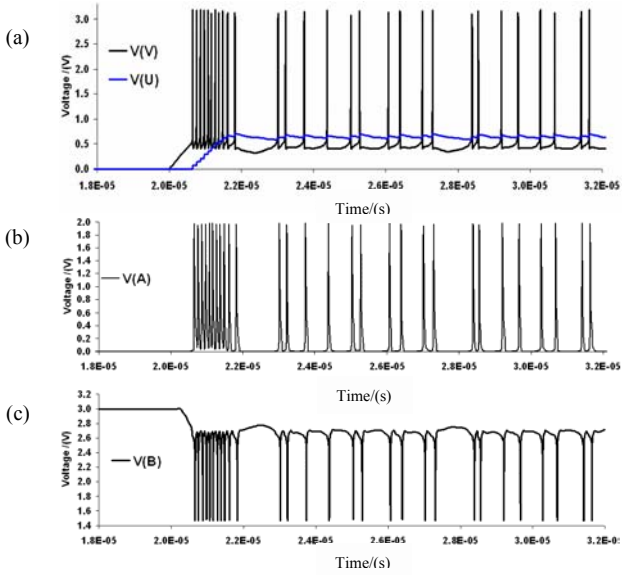


Fig. 3. Waveforms obtained from the sub-circuit shown in Fig. 2:
(a) Example of waveforms of membrane potential, V, and slow variable, U, taken from the circuit shown in Fig. 2(a) and 2(b) respectively. (b) and (c) show V_A and V_B reset pulses generated by the comparator circuit given in Fig. 2(c), when the voltage V is provided as in Fig. 3(a) .

(shown in Fig. 3(c).) as a result M8 is briefly turned on, so that an extra amount of charge is dumped onto C_u, thus increasing the slow variable potential. This amount of increment is determined by voltage V_d.

The comparator circuit is shown in Fig. 2(c). The voltages V_{th} and V_{bias} are the membrane potential threshold voltage and biasing voltage of the comparator, respectively. Once the membrane potential reaches V_{th}, the comparator generates V_A and V_B pulses which are used to reset the membrane potential circuit and the slow variable circuit as shown in Fig. 3.

IV. Phase Plane Analysis of the Circuit

The phase portrait of the proposed circuit is given in Fig. 4 and the phase plane trajectories of CH, IB, FS and RS cells are provided in Fig. 5. These figures were drawn using data obtained from a SPICE simulation in a 0.35µm CMOS technology (CSI from Austria Micro-Systems).

The phase portrait of the circuit, shown in Fig. 4, is obtained without the resetting operation and the direction of resetting is shown using dashed arrows. The resetting circuit becomes active when the membrane potential passes its threshold voltage, V_{th}. However, due to inherent properties of the comparator and MOSFET switching, the resetting operation is delayed by a few ns which allows the membrane to reach a voltage higher than V_{th} before resetting to V_c.

Consider the circuit is biased so that the CH firing pattern is obtained. When a 0.1µA post-synaptic current step is applied to the circuit, the phase plane trajectories and the time domain variations of the membrane potential and the slow variable potential are shown in Fig. 5(a) and Fig. 6 respectively. As seen in Fig. 5(a), initially membrane potential is increased at a higher rate than that of the slow variable potential. The membrane potential reaches its threshold causing resetting circuitry to become active. Consequently, delayed resetting is imposed on the membrane potential, allowing the spike to reach its maximum (≈3.2V) before the resetting pulse discharges the membrane into its resetting voltage, $V_c < V_{th}$, thus completing one cycle of spike generation. When the membrane potential reaches back to its threshold level, the resetting circuit becomes inactive and the membrane starts increasing its potential again, repeating the dynamics of voltage building and resetting (this section is labelled as '**A**' in Fig. 5(a) and Fig. 6). Each spike also increases the slow variable potential U and the spiking continues until the variable U reaches a higher voltage so that the trajectory intersects the V-nullcline. When the V-nullcline is crossed, the orbit follows a new dynamic-route (section '**B**' in Fig. 5(a) and Fig. 6) causing a fast discharge of the slow variable (AHP) until the trajectory reaches the U-nullcline where the rate of increase in V becomes dominant and significant. Once V becomes dominant, since the slow variable U is at a lower potential, it follows similar cycles as the initial section '**A**' but starting at a higher value (section '**C**'). These dynamics repeat as long as the supra-threshold current is sustained and the overall dynamics produce chattering behaviour. The dynamics of the initial phase (section 'A')

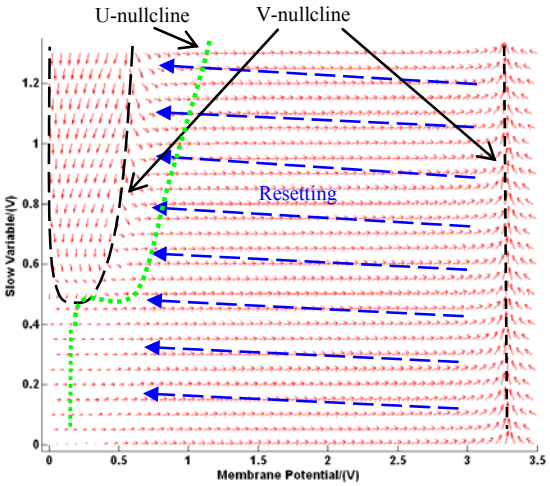
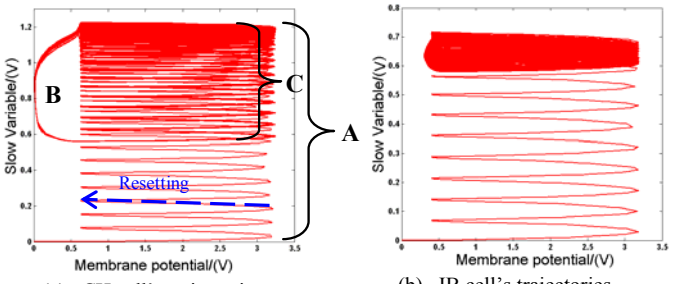
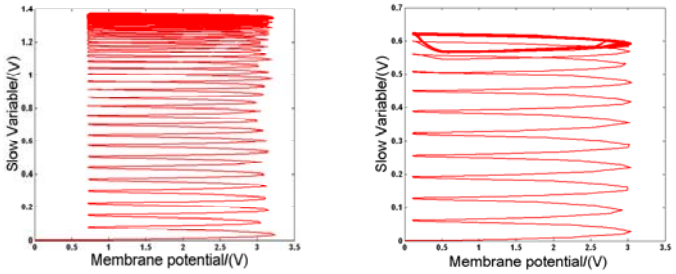


Fig. 4. Phase portrait of the circuit when 0.1µA supra-threshold current is sustained



(a). CH cell's trajectories (b). IB cell's trajectories



(c). FS cell's trajectories (d). RS cell's trajectories

Fig. 5. State trajectories of (a) CH, (b) IB, (c) FS, (d) RS cells when a 0.1µA of postsynaptic current step is injected. (The plots are drawn using data obtained from a SPICE simulation in a 0.35µm CMOS technology)

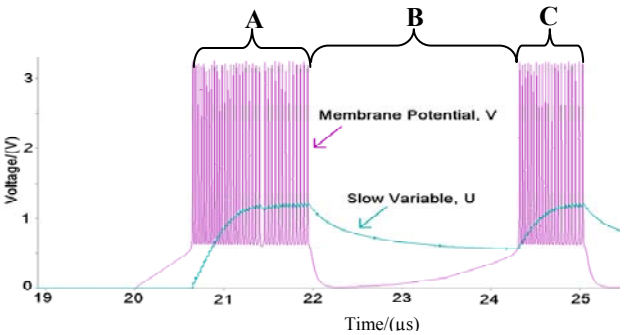


Fig. 6. Response of the CH cell to a 0.1µA post synaptic current step injection showing initial and subsequent spike clusters of the membrane potential and respective slow variable potential. Sections A, B and C correspond to the trajectory in Fig. 5(a).

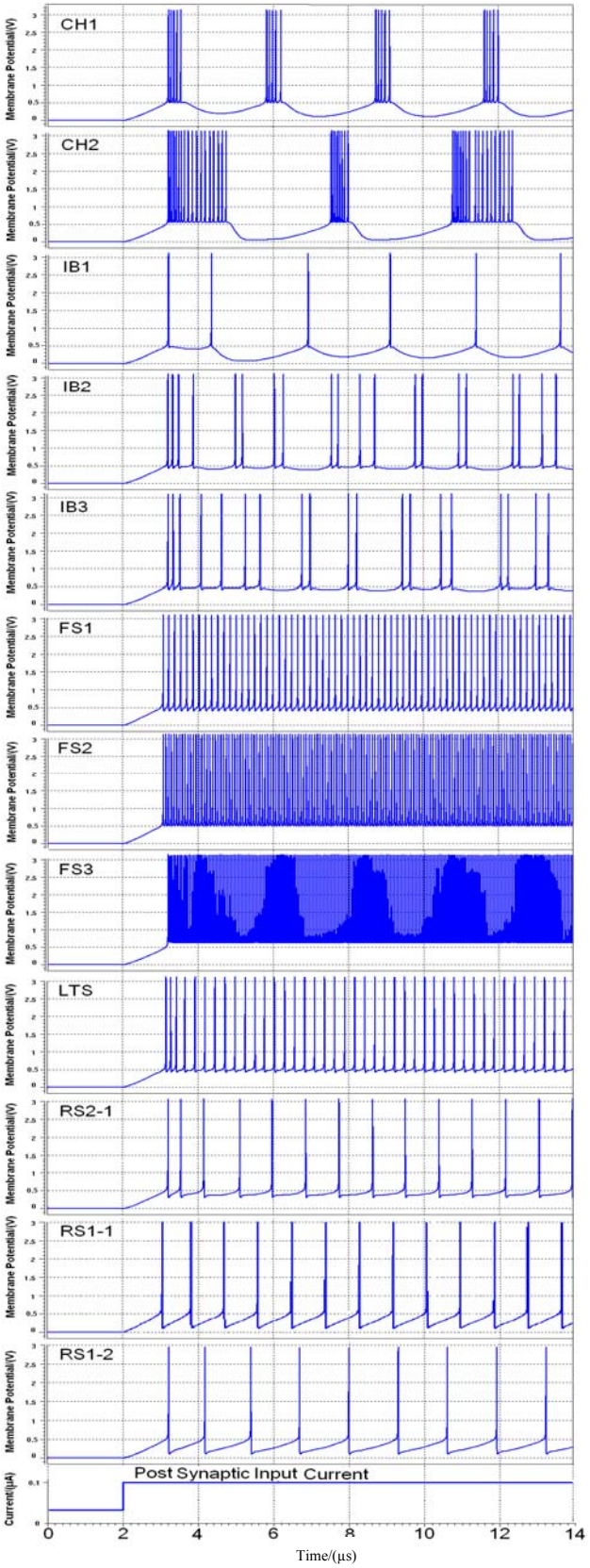


Fig. 7. Waveforms of CH,IB, FS, LTS and RS cells. Each plot shows voltage response of the proposed circuit to a 0.1μA of step current. Parameters V_c and V_d of each response are given in Fig. 8.

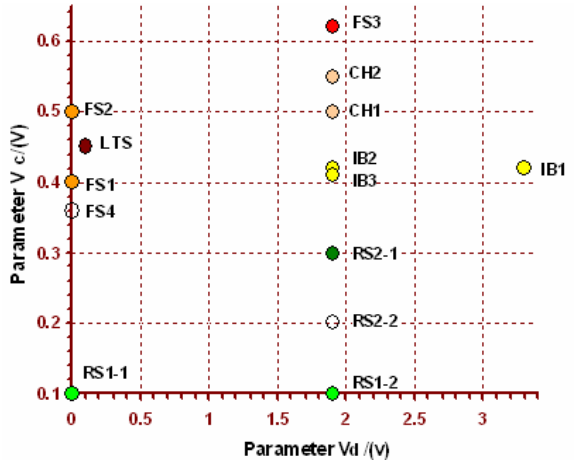


Fig. 8. Values of the parameters V_c and V_d which were used to obtain cortical neuron firing patterns shown in Fig. 7 and Fig. 12 .

Vc /(V)	Corner analysis (worst case analysis)				
	WP	WO	TM	WZ	WS
0.00	RS2	RS2	RS1	RS1	RS1
0.10	RS2	RS2	RS1	RS1	RS1
0.20	IB	IB	RS2	RS1	RS1
0.30	CH	CH	RS2	RS1	RS1
0.40	CH	CH	IB	RS2	RS2
0.50	FS	FS	CH	RS2	RS2
0.60	FS*	FS*	CH	IB	IB
0.65	FS*	FS*	FS	CH	CH
0.70			FS*	CH	CH
0.75			FS*	FS	FS
0.80				FS*	FS*
0.90				FS*	FS*

Fig. 9. Effect of process variation on the value of parameter, V_c required to obtain various behaviours (V_d=1.9V).

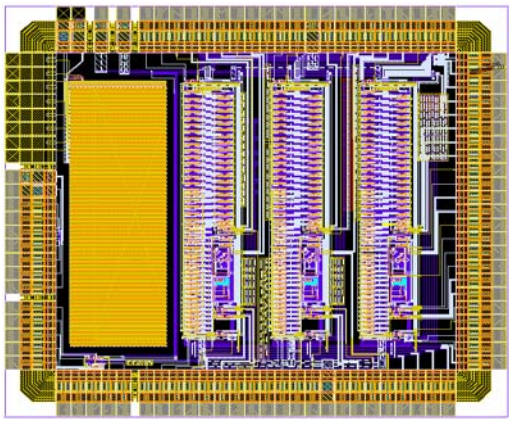


Fig. 10. Chip layout of the neurons

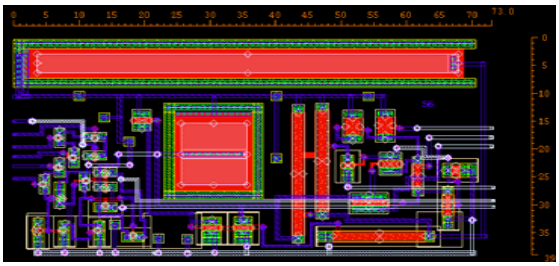


Fig. 11. Layout of the proposed VLSI neuron circuit with the control circuitry and output buffers.

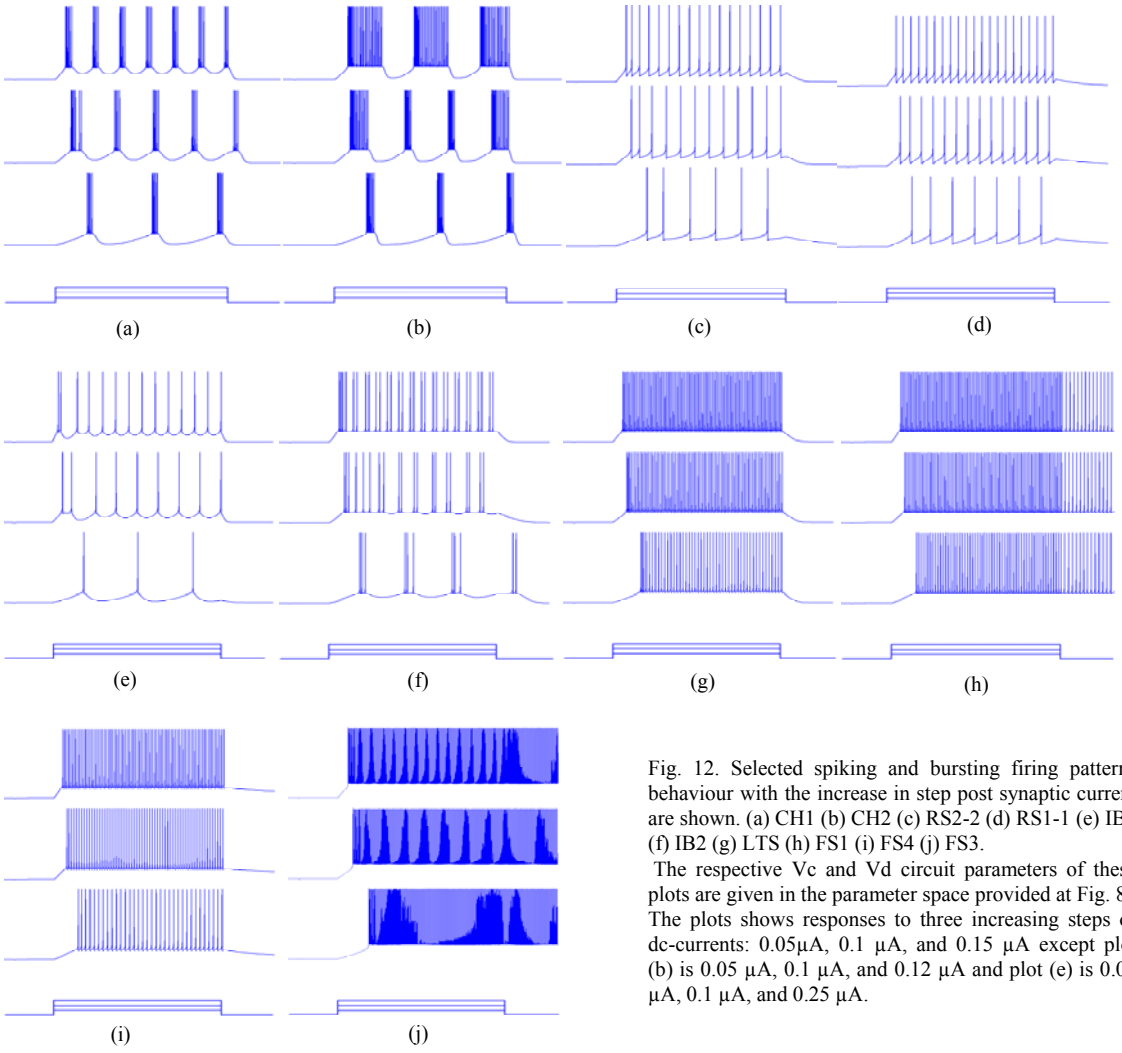


Fig. 12. Selected spiking and bursting firing patterns behaviour with the increase in step post synaptic current are shown. (a) CH1 (b) CH2 (c) RS2-2 (d) RS1-1 (e) IB1 (f) IB2 (g) LTS (h) FS1 (i) FS4 (j) FS3.
The respective Vc and Vd circuit parameters of these plots are given in the parameter space provided at Fig. 8. The plots shows responses to three increasing steps of dc-currents: 0.05µA, 0.1 µA, and 0.15 µA except plot (b) is 0.05 µA, 0.1 µA, and 0.12 µA and plot (e) is 0.05 µA, 0.1 µA, and 0.25 µA.

is responsible for accommodation and the rest corresponds to the steady state dynamics. In a similar way, the IB, FS and RS neurons' trajectories and their dynamics can be explained from the figures shown in Fig. 5(b), (c) & (d) respectively.

V. Simulation Results

The circuit has been designed in a 0.35µm CMOS technology. The post-layout SPICE simulations of the circuit illustrate various types of cortical neuron firing patterns, obtained by changing the values of the circuit variables V_c, and V_d, which are externally controllable. Fig. 7 shows different responses of the circuit to a postsynaptic input current step of 0.1uA; respective parameters of the tuning voltages V_c and V_d are provided in Fig. 8. The circuit parameters of this particular simulation are $(W/L)_{M1}$= (2.3/1), $(W/L)_{M2}$= (2.3/1), $(W/L)_{M3}$= (2.3/1), $(W/L)_{M4}$= (1.3/22), $(W/L)_{M5}$= (5.3/1), $(W/L)_{M6}$= (1.3/18), V_{th} =1.70V, $(W/L)_{M7}$ = (1.3/14), $(W/L)_{M8}$= (1.3/1), V_{dd} = 3.3V, V_{bias} = 0.6V, C_v=0.1pF, C_u=1pF and the typical mean (TM) technology parameter set was used.

As shown in Fig. 9, all firing patterns are obtainable by appropriate tuning of V_c, across four process parameter corners: worst case power (WP), worst case one (WO), worst case zero (WZ) and worst case speed (WS).

The firing patterns of VLSI neurons are on the microsecond scale rather than the millisecond scale of biological neurons. For comparative purposes, all the classifications are done in the scaled time domain in order to adopt biological classifications methods given in [17].

The classification of spiking and bursting firing patterns using inter spike interval histograms obtained from the simulations were presented in [21]. Further, the regular spiking neuron's (RS) frequency of spiking and the accommodation (spike frequency adaptation index) variation with the variation of the postsynaptic input current were also provided in [21] which further illustrated the RS neuron's behavioural similarity with the biological RS neuron.

Variations of firing patterns of selected CH, RS2, RS1, IB, LTS [22] and FS cell types with the variations of postsynaptic current steps are shown in Fig. 12. The respective V_c and V_d parameters of these plots are given in the parameter space in Fig. 8.

It is seen that some fast spiking continues even after the supra threshold current is removed (Fig. 12(h) & (j).) However these cells shut if the inhibitory postsynaptic current is provided. Bursts of three to five spikes are not present in IB1 patterns shown in Fig. 7 and Fig. 12(e). However, reducing the rate of slow variable (U) increase, either by increasing the C_u to C_v ratio (by changing the capacitance) or by reducing the flow of current to C_u (by increasing W/L of M6 or/and decreasing W/L of M7) produces more spikes in the initial burst if required. Using the phase plane analysis of the circuit shown in Fig. 4, the circuit parameters directly related to a certain property of a spike or spike trains can be easily identified. However, it is seen from the phase plane analysis that the flexibility of obtaining IB characteristics is in a narrow range when compared with the other cell classes obtained.

As seen in Fig. 7 and Fig. 12, different known types of cortical neurons are obtained using different values of V_c and V_d. It is also possible to obtain each type of neuron with different characteristics (frequency of spiking and accommodation), changing the width to length ratio of the transistors M4, M6 and M7 [21]. The circuit is capable of representing a wide variety of cell types, and with required accommodation and firing frequency by switching (W/L) of the key transistors. The designed VLSI chip contains a variety of cell designs to experimentally verify these phenomena. Fig. 10 shows the layout of the chip containing 202 neurons with various parameters (transistor sizes and capacitances) that has been submitted for fabrication. The diagram of Fig. 11 shows a layout of a single cell.

VI. Conclusion

The presented compact CMOS circuit is designed using only 14 transistors and it provides flexible switching between different cortical neuron types in a simple way, controlling the external voltages, V_c and V_d. Apart from obtaining different types of neurons, this circuit is also capable of providing a variety of different behavioural cell clusters in each cortical neuron type, with diversity similar to that of real biological neuron cells. The voltage-tuning enables adjustments against process variation. The phase plane analysis of the circuit provides better understanding of the spike dynamics that take place in the circuit which facilitates the identification of circuit parameters directly related to a property of a spike or spike trains. Hence, the circuit provides simple, compact and easily configurable universal cortical neuron for building massively parallel analogue neuromorphic networks that closely resemble the circuits of the neocortex.

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