

ASYNCHRONOUS CELLULAR PROCESSOR ARRAY FOR SKELETONIZATION OF BINARY IMAGES

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Key words to describe the work: Asynchronous processing, self-timed logic, wave propagation, skeletonization, cellular processor array, grassfire transformation.

Key Results: Asynchronous cellular processor array that performs skeletonization of binary images was designed, simulated and tested. Self-timed approach was successfully implemented.

How does the work advance the state-of-the-art?: The design shows how the implementation of asynchronous processing can enhance overall performance of cellular processor arrays in morphological operations.

Motivation (problems addressed): Performance increase in morphological operations that involve “wave-propagation” approach to image processing.

1. Introduction

During the last ten years the “processor per pixel” approach to the design of Cellular Processor Arrays (CPA’s) has attracted significant attention and gained popularity in image processing applications, as it provides high performance, small size and low power consumption compared to conventional vision systems. Most of the CPA’s employ SIMD paradigm and operate in a synchronous mode[1]. However, there are a number of image processing algorithms, such as object reconstruction, hole-filling and skeletonization, which can be implemented in iterative wave-propagation fashion. Asynchronous implementation of such operations, i.e. “single-instruction” realisation, can provide up to N^2 performance increase on $N \times N$ image. Apart from speeding up the execution process such approach is power efficient, because only the active (wave-front) pixels perform logic functions[2].

A hardware realisation of such arrays depends on the algorithm to be performed. If the processing routine consists of a single step – implementation is rather straightforward and employs only combinatorial logic [3]. However, there are a number of algorithms where each processing element (PE) is to accomplish several iterative steps. To implement a design capable to operate without a global synchronization it is necessary to employ the self-timed approach, which implies operation in an asynchronous mode according to the control signals, which are generated internally.

This work presents the design and evaluation of an asynchronous CPA for parallel skeleton extraction in binary images by means of wave-propagation. The processing grid has a hexagonal structure (6 neighbours), as it provides savings in processing time and hardware implementation and avoids an overlapping mesh as compared with 8-connected rectangular grid.

2. Skeletonization algorithm

Skeletonization has been demonstrated to provide a powerful tool for shape representation, object recognition and image compression, where the speed is a critical issue. Most of the existing methods for skeleton extraction are based on iterative thinning. The proposed method has been inspired by the Hildich’s algorithm. In the input binary image a pixel value P_{ij} is assigned to “0” if it is an object pixel and “1” if it is a background pixel. The nearest neighbourhood for every PE is defined as follows:

$N(P_{ij}) = \bigcup_{k=0}^5 \{P_{ij}^k\}$. Let us define three functions:

$$1. B_{ij} = \sum_{k=0}^5 \bar{P}_{ij}^k \quad (2.1)$$

$$2. A_{ij} = |sign(X(i, j) - 1)| \quad (2.2)$$

$$\text{where } X(i, j) = \sum_{k=0}^5 (P_{ij}^k \wedge \bar{P}_{ij}^{(k+1) \bmod 6})$$

$$3. C_{ij} = \prod_{k=0}^5 Y_{ij}^k \quad (2.3)$$

$$\text{where } Y_{ij}^k = P_{ij}^{(5+k) \bmod 6} \vee P_{ij}^k \vee P_{ij}^{(k+1) \bmod 6} \vee A_{ij}^k.$$

Thus the pixel is considered to be not a skeletal point if it satisfies the following conditions:

- 1) $1 < B_{ij} < 6$ - pixel is neither isolated nor internal nor endpoint;
- 2) $A_{ij} = 0$ - pixel is not a junction;
- 3) $C_{ij} = 1$ - prevention of two-pixel lines vanishing.

Each PE has access to the value P_{ij} and A_{ij} of all its neighbours. Initially all the background pixels are activated, and thus propagation starts from object's border and spreads towards its interior.

3. Design and Implementation

The skeleton algorithm has been implemented in asynchronous hardware, employing wave-propagation approach. The CPA consists of 64×64 PE's, arranged in hexagonal way. The PE architecture consists of input latches, combinational circuit for calculating A_{ij} , B_{ij} , C_{ij} , output latches and a control unit, which is responsible for the self-timing of the pixel. The block diagram of the pixel cell is presented in Figure 1. When pixel is activated by any of its neighbours the Control Unit sequentially generates two internal clock pulses.

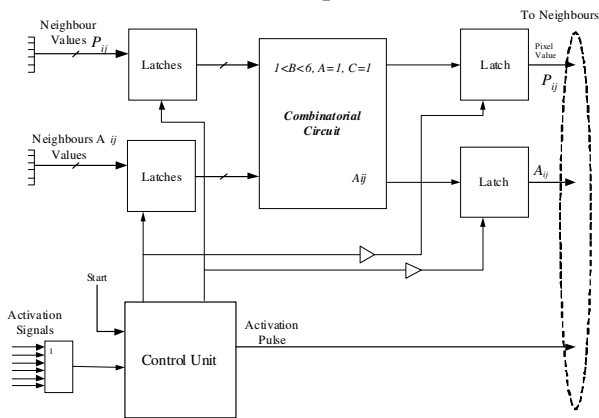


Figure 1: Block diagram of PE

The first pulse updates latches with neighbours' values P_{ij} and then the latch containing pixel's value A_{ij} , the second pulse updates latches with neighbours' values A_{ij} and then the latch with current pixel value P_{ij} . If at any stage of processing the pixel value P_{ij} has been changed to logical 1, then this pixel forms an activation pulse, sends it to all its neighbours and the internal clock generating circuit is set into such a state that the pixel will not respond to any input changes, unless "Start" signal will be set into 1, indicating a new frame. In this way, processors are triggered by their neighbours and perform operations only when required. The activity

spreads across the array in asynchronous, trigger-wave manner, at the maximum speed, determined by the PE's processing time. If the maximum difference in processing time between two PE's activated at the same time is $\Delta t_{\max} = t_{\max} - t_{\min}$, then in order to avoid additional skeletal artefacts the object must not contain the ball of radius $R = \lceil t_{\min} / \Delta t_{\max} \rceil$, which we call a critical size.

4. Design Simulation and Results

The prototype of the chip has been developed and evaluated on Spartan3 xc3s1500 FPGA in order to provide a behavioural proof of the design and estimation of processing characteristics, which are shown in Table 1.

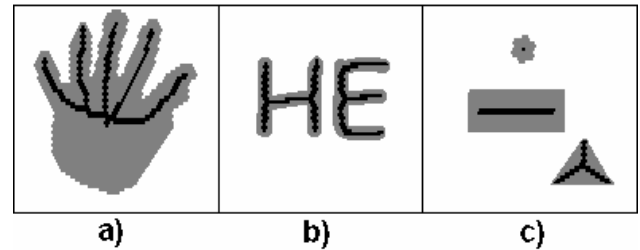


Figure 2: Examples of skeleton extraction

Table 1: Timing characteristics of the Chip

| Max. Processing Time, us | Avg. Layer Eroding Time, ns | Max. Time Difference between two PE's, ns | Max. Frame Rate, frame/s | Critical Size, pixels |
|--------------------------|-----------------------------|---|--------------------------|-----------------------|
| 3 | 103 | 9.8 | 30000 | 10 |

Resulting skeletons contain 2-pixel wide legs, which are a compromise between reliability and speed, and they can be thinned by a single synchronous iteration at the end of propagation.

5. Conclusions

The presented design shows that asynchronous CPA's are efficient in image processing operations that employ "wave-propagation" approach. The described self-timing technique allows implementing asynchronous algorithms that require more than one iteration per PE.

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