Live Demonstration: Real-time image processing on ASPA2 vision system

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***Abstract* — This live demonstration presents a vision system based on a digital SIMD vision chip with in-pixel processing capabilities. The system is comprised of asynchronous/synchronous processor array (ASPA2), embedded custom microcontroller with interface circuits and software development environment. Execution of a number of low and medium level image processing algorithms in real time is demonstrated.**

INTRODUCTION: The presented system features a general purpose vision chip with real-time focal plane greyscale processing capabilities. Despite relatively low resolution such a device delivers high performance, due to massively parallel image processing, coupled with low power consumption. The main application area of the presented architecture is smart surveillance, autonomous robotics and industrial machine vision.

SYSTEM OVERVIEW: The core of the system is 80×80 ASPA2 vision chip [1]. The architecture of the chip is based on an array of bit-serial processing elements arranged in a rectangular grid. Each element is connected to its' four nearest neighbours, so that the neighbour's data can be accessed in both synchronous and asynchronous fashion. The array operates according to the SIMD paradigm, where every cell executes the same instruction broadcast by a central controller, which in the presented setup is implemented off-chip on the FPGA. Each cell operates as a simple microprocessor with added functionality to support global asynchronous data-processing. The processing element comprises a register file, bit-serial ALU with a shift register, a photo-sensor with one bit A/D converter and I/O port for multiplexing input data. The functionality of the cell is expanded by a 'propagation chain', which enables global asynchronous trigger-wave data propagation. The topology of such propagation network is constrained by local data in every PE. In addition to the processor array, the vision chip comprises additional peripheral circuitry that further expands overall functionality. An addressing unit supports three pixel addressing modes: random pixel access, block and fixed pixel pattern modes. To enable global arithmetic operations, ALUs of the neighbouring cells in one row can be chained together and configured as a single ripple-carry adder. The row-wise sub-sums are combined in a column parallel adder, which enables asynchronous global summation. Finally, the chip operation is enhanced with asynchronous address extraction mechanism that facilitates extraction of top, bottom, left and right coordinates of segmented objects. It also enables address-event based (AER) read out mode.

At 75MHz the 80×80 ASPA2 vision chip delivers 15.3 GOPS (greyscale), 240 GOPS (binary) and 1.9 GOPS (unsigned products/quotients) in synchronous mode, with 373 GOPS/W power efficiency. The overall performance figures can be further improved by taking into account asynchronous operating mode. The chip features an 8-bit parallel data interface with 18 MPixel/second output throughput.

TRACK: Sensory Systems / Imagers and Vision Processing.

DEMONSTRATION SETUP AND VISITORS EXPERIENCE: The demonstration consists of a camera with the ASPA2 vision chip and a laptop with computer screen for visualization. The camera visual output is displayed on the screen. Additional data such as frame rate, coordinates of extracted objects and other statistical information is also displayed. The camera communicates to the PC via USB interface. Displayed in Figure 1 is a test system and the ASPA2 chip microphotograph. For the demonstration a new more compact (80×50 mm^2) version will be presented.

Visitors will learn about smart image sensors and benefit of massively parallel in-pixel processing. They will also be introduced to advantages of global asynchronous operations. Furthermore, all aspects of parallel programming for cellular processor arrays will be presented utilizing Array Processing enviRONment (APRON) software [2]. The visitor will be able to dynamically upload various image processing programs into the system, control the execution in real-time by means of adjustable parameters and manually modify simple programs to understand the operation principle and observe the immediate feedback from the vision system.

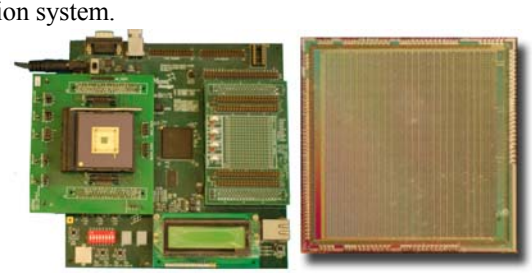

Figure 1: Current test system and 80x80 ASPA2 vision chip.

REFERENCES:

[1] A. Lopich, P. Dudek, "An 80x80 general-purpose digital vision chip in 0.18 um CMOS technology," *IEEE International Symposium on Circuits and Systems*. pp. 4257-4260, 2010.

[2] D. R. W. Barr, P. Dudek, "APRON: A Cellular Processor Array Simulation and Hardware Design Tool," *EURASIP Journal on Advances in Signal Processing,* vol., 2009.