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Integrated Circuit Implementation of a Compact Discrete-Time Chaos Generator

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Abstract. A discrete-time chaos generator implemented with two nonlinear circuit cells has been fabricated in a 0.6 μm CMOS technology. Each cell is creating a function (map) which allows a chaos signal to be generated. Measurements of the chip were performed with a supply voltage of 5 V, up to a frequency of 2.5 MHz. A bifurcation diagram of the circuit and the Lyapunov exponent calculation are presented. The size of the generator layout (without the switches) is 32×19 μm which makes it suitable for applications where many chaos signal generators are required on a single chip.

Key Words: map circuit, chaos generator, bifurcation diagram, Lyapunov exponent, random noise generator

1. Introduction

Integrated circuit implementations of non-linear deterministic systems, which display chaotic behaviour, have been a subject of continuing research during the last decade [1–5]. The importance of these circuits became more evident with the development of chaos communications and chaotic neural networks [6, 7]. Discrete-time chaos circuits generate a chaotic series through an iterative application of a suitably chosen non-linear function (or chaos map), as follows:

$$f : R \to R \quad x_{n+1} = f(x_n) \tag{1}$$

Generally, the chaos circuits are designed to implement one of the known chaos maps in order to be able to create a chaos signal [8]. The map we use here is an approximation of a V-shaped map and is created by a three-transistor circuit cell introduced in [9]. We have implemented an integrated circuit chaos generator, which comprises two such maps introduced in a closed loop, having a total of 10 CMOS transistors, 4 of them creating the necessary switches, and no additional capacitances; this helps to achieve a compact layout. In this paper the chip design and measurement results are presented. The chaotic operation of the circuit is verified experimentally, as indicated by the bifurcation diagram and the positive value of the Lyapunov exponent.

2. Map Circuit

A one-dimensional map is the simplest way of achieving a random-like signal. To generate a discrete-time chaotic signal a system with a delay circuit block (sample and hold circuit) and the nonlinear circuit (map circuit) placed in a loop is created [3]. The map circuit is required to implement a nonlinear characteristic, with the "average" slope of its branches greater than unity.

Many non-linear functions suitable for chaos generation are known. In particular, chaos maps can be achieved with V-shape functions [8], but the branches can be described by a different function, not necessarily a linear one and still creating a V-shape characteristic, which allows some degree of freedom in constructing the map circuit. This is especially true for some applications, such as stochastic neural networks, where accuracy of the map function, and consequently particular frequency spectrum or statistical properties of the generated signal are not as important as its general random-like quality. In such case, very simple map circuits can be employed. A V-shape can be constructed with two circuits; the function thus achieved will be the *DC*-characteristic of the final map circuit. The first circuit can be a common-source amplifier, which generates the branch of the function with the negative slope and the second one can be a source follower, which creates the branch with the positive slope. Note that both of the circuits must be connected in parallel, so that the "summation" of their *DC* characteristics is achieved. A circuit implementing such a characteristic, introduced in [9], is shown in Fig. 1.

Here, the transistor M_3 plays the role of the source follower (with M_1 as load) and the transistor M_1 is acting as the common source amplifier (with M_2 as load). The two "sub-circuits" share the same input and the same output, thus creating the transfer characteristics as shown in Fig. 1. The characteristic can be adjusted by changing the value of the bias voltage V_B.

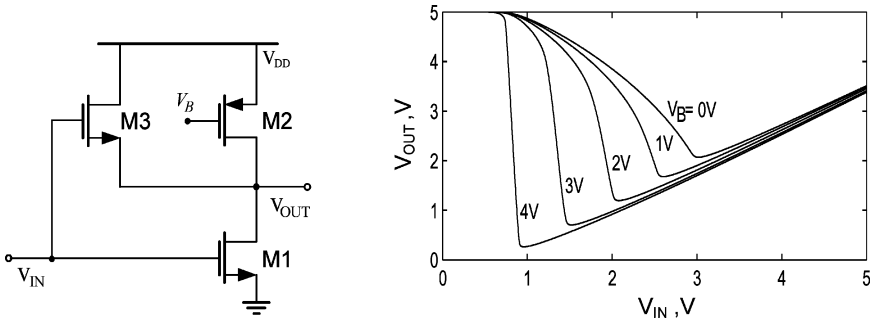

Fig. 1. Map circuit [9] and its DC characteristic.

To explain the operation of the circuit let us consider that V_{IN} is being slowly increased from 0 V. Notice that the transistor M_3 turns on later than the transistor M_1, so initially the negative slope of the characteristic is created (following the DC characteristic of the inverter composed of M_1 and M_2). As V_{IN} increases and V_{OUT} decreases, at some point M_3 starts to conduct and the positive part of the characteristic begins to be generated. The transistor M_3 acts as a source follower, but its biasing current, provided by M_1, keeps increasing. To ensure that the slope of the positive branch is close to unity, the W/L ratio of M_3 should be much greater than that of M_1. The values of the transistors used in the fabricated circuit are as follows: $M_1 = 4\ \mu\mathrm{m}/0.6\ \mu\mathrm{m}$, $M_2 = 4\ \mu m/0.6\ \mu\mathrm{m}$, $M_3 = 40\ \mu m/0.6\ \mu\mathrm{m}$

3. Chaos Generator Circuit

Usually, the implementation of a discrete-time chaos generator requires two sample-and-hold (S/H) circuits in addition to a map circuit. The circuit which has been fabricated here follows an alternative solution [9] to the standard configuration and it is given in Fig. 2.

It can be seen that this circuit is made of two map circuits (the circuits in Fig. 1 are used) and two sample-and-hold circuits which consist of switches and the capacitors C_1 and C_2. Every switch is implemented with a pair of transistors (nMOS and pMOS), but the capacitors do not actually consist of separate physical devices; they are in fact the input capacitances of the map circuits I and II. This eliminates the need for additional capacitors, thus saving the silicon area required.

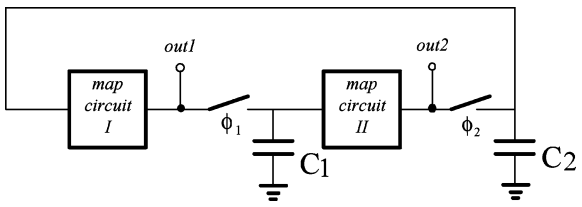

Fig. 2. Chaos generator.

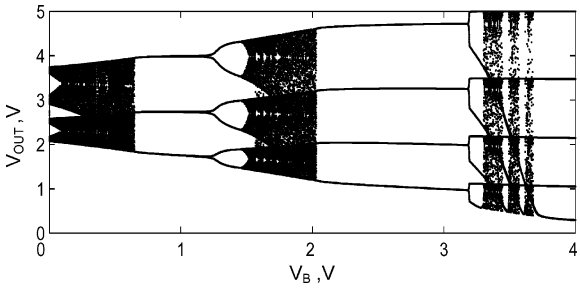

Fig. 3. Simulated bifurcation diagram of the chaos generator.

Figure 3 shows the bifurcation diagram of the simulated generator circuit, obtained by plotting 5×10^4 output signal samples when V_B was swept between 0 V and 4 V. Because both of the map circuits contribute to the generated chaos series, the outputs out_1 together with out_2 form the complete bifurcation diagram. As it can be seen, regions of chaos and windows of periodic behaviour of the circuit are present. It should be noted, that in a physical implementation the two map circuits will never be exactly identical, due to component mismatch. Nevertheless, the resulting composite mapping function will still lead to a chaotic behaviour.

4. Experimental Results

4.1. Physical Implementation

We have implemented the chaos generator circuit in a standard 0.6 μm CMOS technology. Figure 4 shows a microphotograph of the fabricated chaos generator with details about the circuit blocks.

Two map circuits occupy an area of $32 \times 19\ \mu$m while the switches in this particular layout are implemented with two transistors (nMOS and pMOS) and are placed together with inverters adjacent to the map circuits. For an even more compact implementation single-transistor switches could be used.

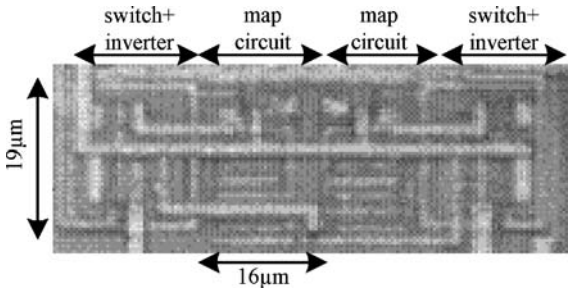

Fig. 4. Microphotograph of the fabricated chaos generator.

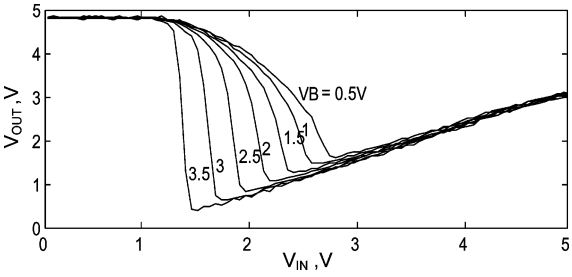

Fig. 5. Measured DC characteristics of the map circuit.

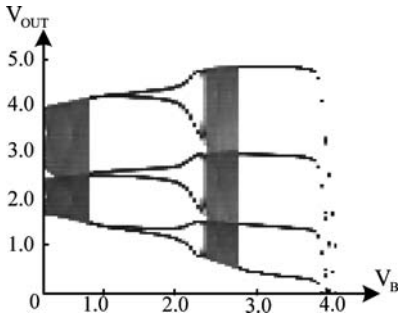

Fig. 7. Bifurcation diagram of the fabricated circuit.

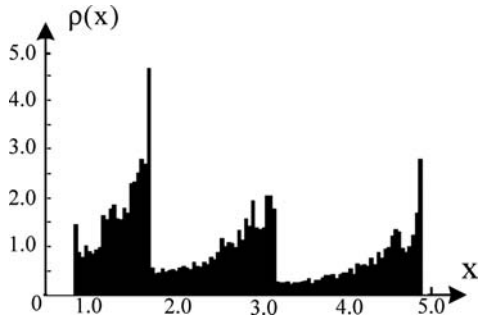

Fig. 8. The distribution function of the output voltage samples for $V_B = 2.65$ V.

4.2. Measurement Results

The measurements were performed using standard laboratory instruments. The measured *DC* characteristics of the map circuit for different control voltages V_B are given in Fig. 5; they resemble the simulated DC characteristics in Fig. 1.

For different bias voltages chaotic ($V_B = 0.8$ V) and periodic ($V_B = 2.5$ V) output signals were observed on the oscilloscope, as shown in Fig. 6.

The bifurcation diagram shown in Fig. 7 was obtained using 10^5 samples of measured output signals for each value of the voltage V_B, swept in discrete 0.1 V intervals between 0 and 4 V. Voltage samples at both outputs, out_1 and out_2, were recorded. The grey-level intensity of the "pixels" in the diagram corresponds to the number of output voltage samples recorded in the particular voltage range. As verified in the simulations, one can observe regions of chaotic and periodic behaviour of the circuit.

Figure 8 shows the measured distribution $\rho\ (x)$ of the output voltage samples for the bias voltage $V_B = 2.65$ V. The distribution is not uniform, but it can be seen that the voltage samples are distributed densely along the output range.

4.3. Lyapunov Exponent

To further analyse the generated series the Lyapunov exponent can be calculated. A positive Lyapunov exponent indicates that the generated series is chaotic. This exponent is defined by the following equation:

$$\lambda = \int \log |f'(x)| \rho(x)\, dx \qquad (2)$$

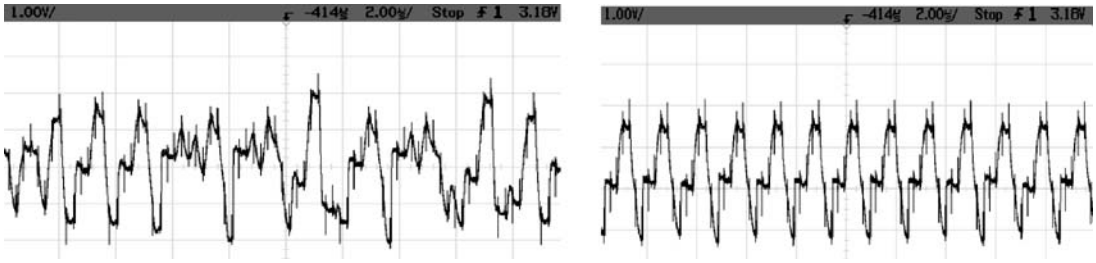

Fig. 6. Chaotic and periodic signals observed at the output of the fabricated circuit with clock frequency of 2.5 MHz.

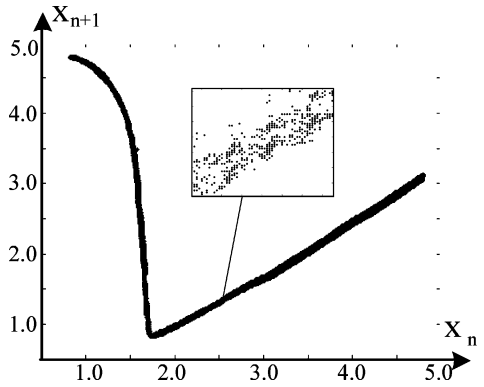

Fig. 9. The map of the fabricated circuit obtained using the experimentally observed output voltage samples for $V_B = 2.65$ V. The inset shows a magnified part of the map.

However, the above definition assumes, that the function $f(x)$ and the distribution function are known analytically. In our case, we need to estimate the value of the Lyapunov exponent numerically, based on the samples of the output voltages obtained experimentally, for each particular value of parameter V_B. For this purpose the map is plotted, using experimentally obtained pairs of output voltage samples (x_n, x_{n+1}), as illustrated in Fig. 9. The measured map is noisy, so the data needs to be averaged. The output range x is divided into I intervals Δx_i, and the discrete values of the distribution function $\rho(x_i)$ and the map gradient $\Delta f(x_i)/\Delta x_i$ are calculated numerically for each interval. The Lyapunov exponent is then calculated according to the following equation:

$$\lambda = \frac{1}{I}\sum_{i=1}^{I} \log\left(\left|\frac{\Delta f(x_i)}{\Delta x_i}\right|\right)\rho(x_i). \tag{3}$$

A plot of Lyapunov exponent values, calculated for various values of V_B is shown in Fig. 10. It has to be noted that the calculated values are only available in case the generated signal has a dense distribution function, i.e. in a non-periodic case. It should be also emphasised, that the method used for calculations uses averaging, thus smoothing out the noise components, but also potentially affecting the accuracy of the calculated Lyapunov exponent. Nevertheless, in this case we do know that the random signal at the output of our generator circuit is a result of a deterministic process of map iteration (even though it might be affected by noise) and this is confirmed by a positive Lyapunov exponent, which indicates that the series is chaotic. For instance, for $V_B = 2.65$ V the Lyapunov exponent was calculated as being equal to 0.1212.

4.4. Frequency and Power Supply Considerations

The main two factors that limit the functionality of the circuit are the frequency of operation and the power supply needed to generate chaos or periodic signal.

Measurements on the chip showed that the behaviour of the circuit is constant up to the maximum operating frequency of approximately 2.5 MHz. For higher clock frequencies the output of the generator can still be chaotic, but the amplitude will decrease, and the dynamic behaviour of the circuit will become more complicated due to the fact that the sample-and-hold capacitances will not be fully charged/discharged during the clock period. The measured operating frequency has been limited mostly by the bonding pads and off-chip capacitances. The simulations have shown that the core circuit cell can operate at much higher frequencies and it ceases to behave chaotically above a frequency in the region of 900 MHz. The simulated bifurcation diagrams of the circuit for different clock frequencies are shown in Fig. 11. The circuit was operated with a 5 V power supply voltage and the total power

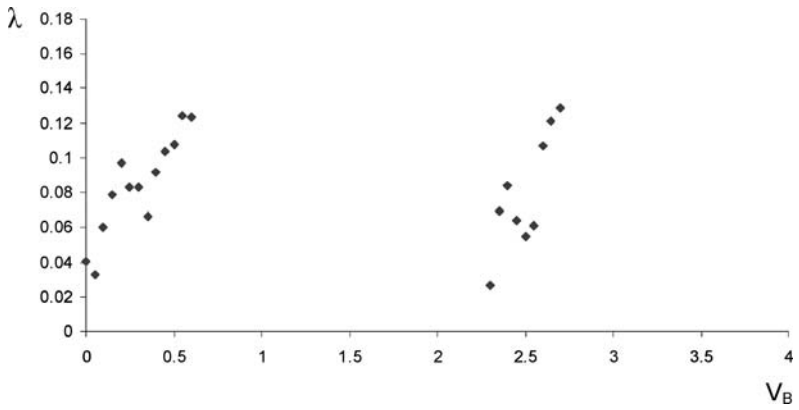

Fig. 10. Calculated values of the Lyapunov exponent for various values of V_B.

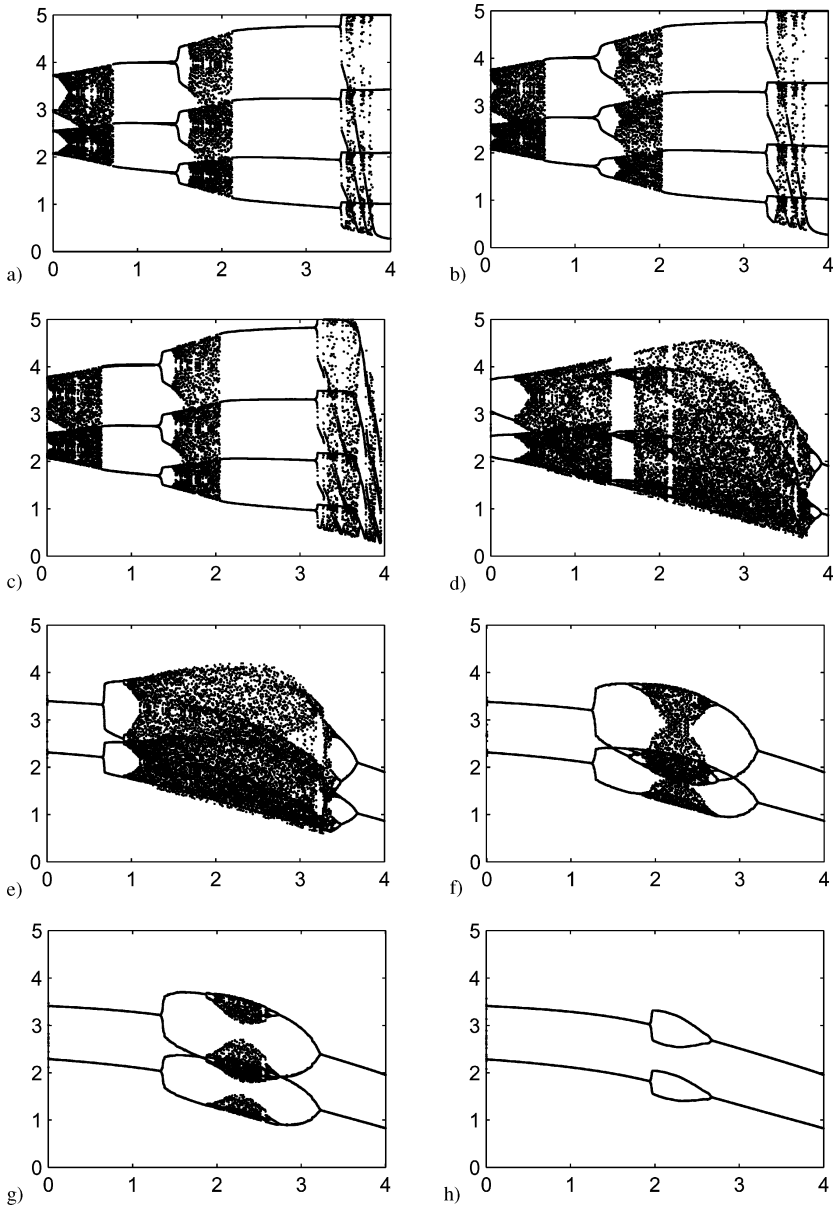

Fig. 11. The simulated bifurcation diagrams for different clock frequencies: (a) 100 kHz, (b) 10 MHz, (c) 100 MHz, (d) 500 MHz, (e) 700 MHz, (f) 900 MHz, (g) 1 GHz, (h) 1.1 GHz. For all the diagrams the x-axis is the control voltage V_B and the y-axis is the output voltage V_{OUT} ; all the voltages are given in volts.

consumption was measured to be equal to 7.85 mW. The relatively large power consumption is mostly due to the fact that for large input voltages V_{IN} there is a relatively large current flowing from V_{DD} to ground (through M_3 and M_1). This could be a problem if a very large number of chaos generators were required on a single chip and this issue should be addressed by further research.

5. Conclusions

A compact chaos generator, based on a three-transistor chaos map circuit, has been designed and implemented in a 0.6 μm CMOS technology. The operation of the circuit has been verified experimentally. The circuit generates chaotic series, is simple and robust, occupies a very small silicon area and could be thus easily replicated to provide multiple uncorrelated random signal sources on a single chip. It is suitable to be used as a noise source in a sensory system design [10] or in stochastic neural networks and similar applications.

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