A Zero Dead-Time, High Temporal Resolution, Time-of-Flight Particle Detector IC.

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Abstract: ***This paper describes principles of the design of a CMOS time to digital converter integrated circuit, intended for time of flight spectrometry applications. The chip utilizes the differential delay line technique to achieve 150ps accuracy, and a novel read-out circuitry which allows the achievement of dead-time less operation.***

1.INTRODUCTION.

This paper describes progress that has been made on work first reported at EUROSENSORS X, [6]. At that time a prototype integrated circuit was described which used a 32-phase clock to record the arrival time of incident particles. The chip architecture was such that data could be acquired continuously to a timing resolution of 1ns and up to a peak input frequency approaching 500MHz.

Modern time of flight (TOF) spectrometry systems, used in particle physics experiments as well as in industrial methods of material surface analysis (Secondary Ion Mass Spectrometry, SIMS)[1] require not only a resolution well below 1ns, but also a low dead-time (i.e. the minimum time between two measurements).

Diverse methods of digitizing of short time intervals has been proposed, ranging from fast counters [2], through analog methods based on generating a voltage ramp [3], to various CMOS tapped delay line configurations [4]-[6]. The delay line method is of a particular interest, since unlike the other methods, requires nothing more than a standard digital CMOS process. This has the advantages of a relatively small cost, low power dissipation and high integration level. The high resolution is obtained by utilizing a logic buffer delay as a time unit, and a Delay Locked Loop (DLL) is used to stabilize the value of the buffer delay against process variations, temperature and power supply changes. Because the system must be designed to work properly in a "worst case" the resolution obtainable in contemporary CMOS processes is limited to around 500ps. The improvement of the resolution can be achieved by using a differential method.

The differential delay line was described in [4], and resolutions down to 100ps have been shown to be obtainable in a pulse-shrinking delay line. The other interesting method of improving the resolution of DLL is based on an array of delay lines, and was described in [7]. However both the pulse-shrinking, and the array approaches have an inherent burden of a long dead-time (allowing for only one measurement per clock cycle). The

differential delay line technique allows for a dead-time less operation, but a special read-out method is necessary.

2. DIFFERENTIAL DELAY LINE.

In a differential delay line method two delay buffer chains are used. The basic configuration is illustrated in Fig.3. The concept is similar to the vernier method. The delay of a buffer in the upper delay chain t_1 is slightly greater than the delay of a buffer in the lower delay chain t_2. The time unit t_R is defined as (t_1-t_2). The time difference between the START and the STOP pulse is decreased by each differential stage by t_R. The position in the differential delay line at which the STOP signal catches up with the START signal, gives therefore an information about the measured time, with the resolution of t_R. This can be determined by detecting a HI/LO transition in an output word, Since t_R is equal to a difference between the delays of two buffers, it can be made very small. In practice the time resolution will be limited by error factors, like mismatch of the transistors and noise.

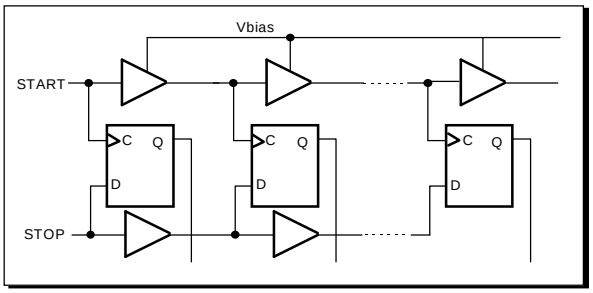

Fig.3. Differential Delay Line.

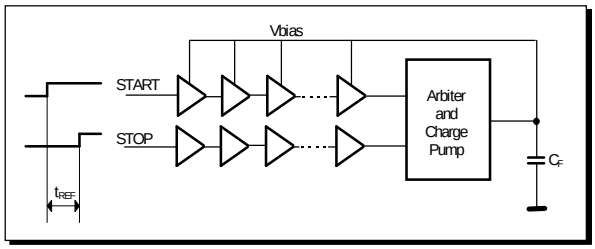

Fig.4. Delay Locked Loop stabilizing differential delay.

To make a time unit t_R insensitive to process variations and ambient conditions, the time difference between delays of two chains is locked to a reference time period t_{REF} by a DLL (Fig.4.), and one of the buffer chains is constructed from voltage-controlled buffers. For N buffers long delay line the resolution will be equal to

$$t_R = (t_1-t_2) = t_{REF}/N \qquad (1)$$

For voltage-controlled delay buffers we used the design depicted in Fig.5 ([5],[6]). For non-controlled buffers we use just two inverters in series. By appropriate dimensioning it is ensured, that in any conditions the differential delay of 150ps may be achieved for some V_{BIAS} value. The simulated characteristics are presented in Fig.6.

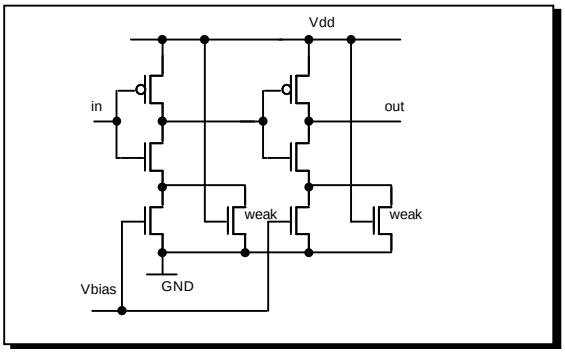

Fig.5. Voltage-controlled buffer

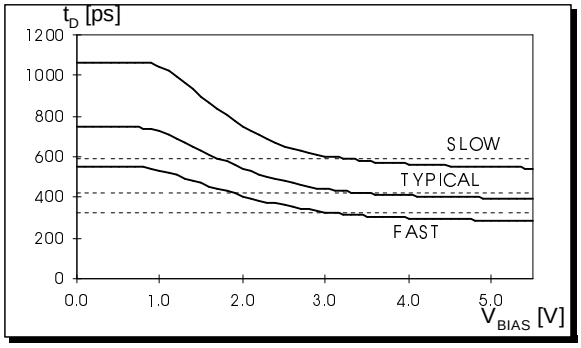

Fig.6.Delay vs bias voltage characteristics in extreme cases (Process=fast,typical,slow;Vdd=5.5,5.0,4.5V;T=20,80,120°C)

3. DEAD-TIME LESS OPERATION.

When the reference maximum time measured by a differential delay line is equal to a clock period T_C the dynamic range of a system can be easily expanded, by counting clock pulses. The counter gives a coarse timing information. The delay line is used to give fine timing information, within one clock period.

To measure the time difference between the clock edge, and a certain event (i.e. the arrival of a particle at the detector in a TOF spectrometer), the START input of a differential delay line is driven by a clock signal, and the events are signaled at the STOP input. However, since the delay of a buffer t_1 is longer than a time resolution t_R, the propagation time of the clock signal through the delay line t_{prop} is greater than the clock period .

$$t_{prop} = N \cdot t_1 > N \cdot t_R = T_C \qquad (2)$$

This means, that one clock pulse starts to propagate in a delay line while the previous ones are still propagating. Moreover, to achieve a dead-time less operation, we have to enable for multiple STOP pulses propagating at the same time in the delay line. That leads to the situation, where there is no single moment in time, when we could read the outputs of all delay line latches.

This problem is solved by reading-out partial results, and passing them through a register pipeline as depicted in Fig.7.

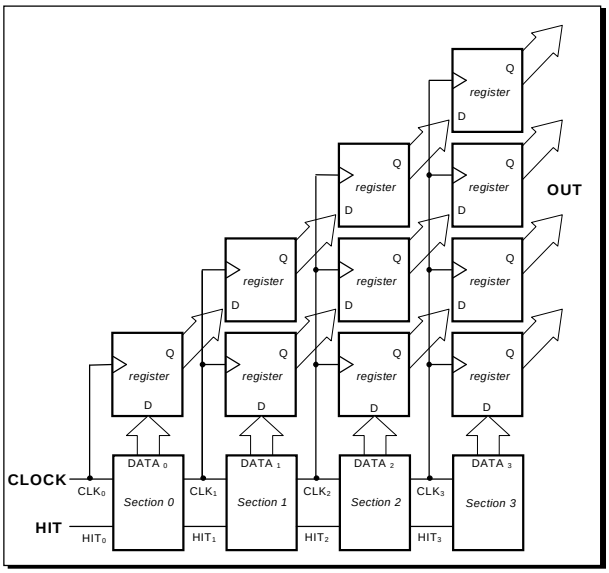

Fig.7. Read-out scheme. For clarity of the picture the system with k_{SECT}=4 sections is shown.

The differential delay line is divided into k_{SECT} sections. Each section works as an "independent" differential delay line, and it is effectively resolving STOP signals that come in a certain time-window of a global clock period. At the output of each section START and STOP pulses are skewed by the time-window width of $N/k_{SECT} \cdot t_R$.

Because the propagation time through the section is k_{SECT} times shorter than a propagation time through the whole differential delay line, it can be ensured, that all the delay line latches of one section are latched at some instant. At this instant the outputs are latched into pipeline registers.

If we use level-sensitive latches it has to be ensured, that the worst case CLOCK signal delay through the section should be smaller than a half of the clock period (with a suitable margin for set-up of the latches etc). As a general guideline it must be observed, that

$$t_{1max}/t_R \cdot k_{SECT} < 1/2 \qquad (3)$$

This can be easily achieved by appropriate dimensioning of the transistors, and by choosing adequate section lengths.

The sections are clocked by delayed clocks, and if expression (3) is observed it is also ensured, that when the results from one section are latched, the pipeline registers from previous section still contain the timing information from the previous time-window of the same clock cycle. The information is passed through the pipeline as the CLOCK signal travels along the delay line.

In this way, at the output of the register pipeline there is a full timing information about the STOP pulses in one clock cycle, updated every cycle. That leads to a dead-time less operation. Coarse counter data can be then easily appended.

4. CHIP DESIGN.

The integrated circuit built on the above principles was designed in 0.7μm technology. The measurement system (i.e. the differential delay line, the register pipeline and the DLL) was designed in full custom. The layout has to be performed very carefully, to minimize the nonlinearities. In particular, the delay line must be laid out as an unbroken chain of identical inverters, and the mismatch of the transistors must

be minimized (e.g. by using relatively large area transistors). The guard-rings must be introduced to minimize the noise coupled through the substrate.

To obtain t_R=150ps accuracy the delay line is N=128 elements long, and the clock frequency T_C=52.08 MHz. The delay line is divided into k_{SECT}=16 sections.

The integrated circuit design includes also a data reduction mechanism, to counteract for the great amount of mostly trivial data, obtained by a chip in a spectrometry application. The chip architecture is presented in Fig.8.

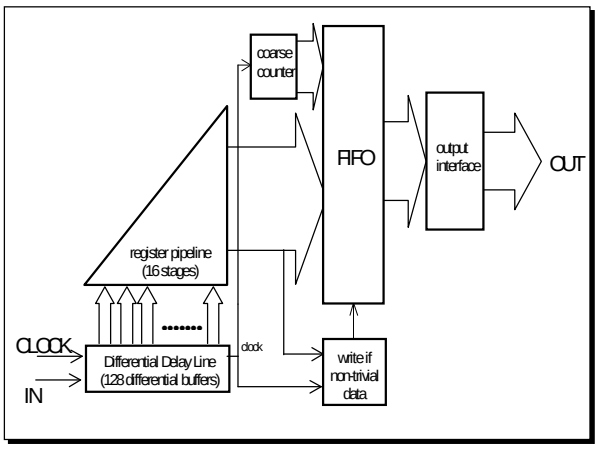

Fig.8. Chip architecture.

Whereas the chip is mainly digital, the design of the DLL and the voltage-controlled buffers involves analogue techniques. All the subcircuits designed in full custom were simulated using HSPICE. Data buffering and output interface subsystems were designed using standard cells. The whole system was successfully simulated using the Verilog-XL logic simulator.

5. CONCLUSION.

Performed simulations proved the correct operation of the system. The dead-time less operation with the 150ps time resolution was achieved in a differential delay line structure.

There are several factors, that limit the accuracy of the differential delay line. The mismatch of the transistors in the buffers leads to the mismatch of the buffer delays, which in turn leads to the nonlinearities of conversion. Also the noise in circuits can be a source of a timing jitter. This is a subject of our present research. The test-chip is currently being fabricated, which will allow the measurement of actual nonlinearities of conversion in a Differential Delay Line based TDC.

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