Compact discrete-time chaos generator circuit

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A three-transistor CMOS circuit is presented, with adjustable nonlinear characteristics, which can be used as a map that generates discrete-time chaotic signals. A method of constructing a chaos generator using two map circuits is also proposed. The circuit is very compact, which makes it suitable for applications requiring the integration of a large number of random signal generators on a single VLSI chip.

Introduction: A discrete-time chaotic series can be generated by a simple iterative procedure:

$$x_{n+1} = f(x_n)$$

where $f(x)$ is a suitably chosen nonlinear function, operating here as a one-dimensional map. Recently, several analogue circuits generating discrete-time chaotic signals have been proposed [1–3]. These circuits are usually carefully designed to approximate one of the well-known chaos maps, e.g. a tent map or a logistic map, in order to obtain required statistical or frequency properties of the generated signal. There are applications, however, where these properties of the chaotic signal are of lesser importance, as long as the signal remains aperiodic and unpredictable. However, physical parameters of the circuit such as its power dissipation or the size of implementation may be of greater importance. This is particularly true if a large number of chaos generators are required on a single integrated circuit, e.g. to act as annealing noise sources in a stochastic neural network [4]. Similar considerations apply to the design of chaotic neuron circuits [5]. In this Letter we demonstrate how a compact three-transistor CMOS circuit can be used to implement a nonlinear map suitable for chaos generation. We also propose a compact chaotic signal generator consisting of two map circuits.

Map circuit: In general, a chaos map circuit is required to implement a non-monotonic characteristic, with the 'average steepness' (averaging in terms of the probability distribution of the generated chaotic signal) greater than unity. The proposed map circuit, which achieves this requirement, is shown in Fig. 1. The transfer characteristics of the circuit, for various values of the bias voltage V_{BIAS}, are shown in Fig. 2. The operation of the circuit is briefly as follows. For input voltages V_{IN} less than the threshold voltage of M_1 the output V_{OUT} is at V_{DD}. The transistor M_3 is cut-off. As V_{IN} is increased the voltage V_{OUT} starts to decrease, following the transfer characteristic of an inverter composed of M_1 and M_2 (with the slope determined by the relative sizes of M_1 and M_2, as well as the voltage V_{BIAS}). At some point, the voltage V_{OUT} falls below V_{IN}, so that the gate-source voltage of M_3 becomes larger than its threshold voltage and this transistor starts to turn on. Consequently, further increase in V_{IN} leads to the increase in V_{OUT} due to the 'source follower' operation of M_3. (The current through M_1 keeps increasing, but the slope of the V_{OUT} against V_{IN} characteristic can be close to unity if the transistor width to length ratio of M_3 is much larger than that of M_1.)

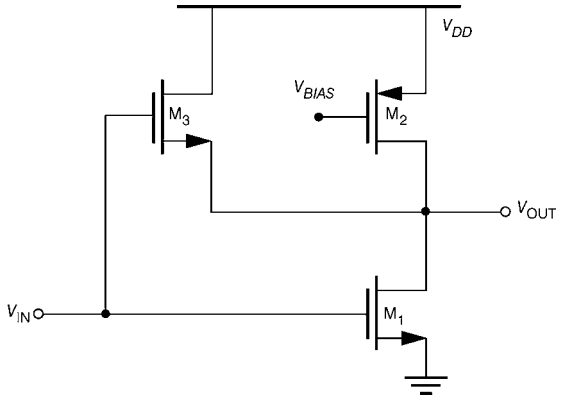

Fig. 1 *Proposed map circuit*

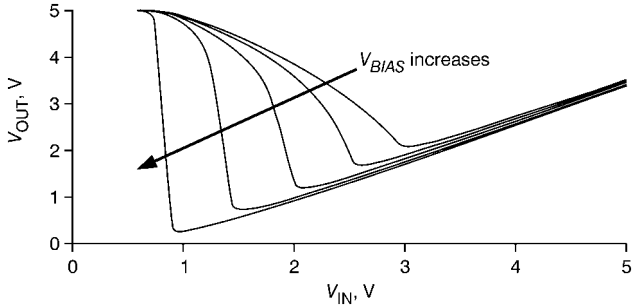

Fig. 2 *DC transfer characteristics of proposed map circuit*

It is important to make sure that the map circuit design is robust against process parameter variations, which may affect the steepness of the characteristic. In our circuit, the map characteristic may be adjusted by changing the voltage V_{BIAS}. In the generator this will determine whether the output signal is chaotic or periodic. This controllability is essential for applications such as chaotic neural networks.

Chaos generator: Normally, in addition to a map circuit, two sample-and-hold (S/H) circuits are required to implement a discrete-time chaos generator. In a voltage-mode circuit, assuming that the map circuit has a high-impedance input, the arrangement shown in Fig. 3*a* should be used. A two-phase clock is required. On phase ϕ_1 the input of the map circuit is equal to x_n, the map circuit evaluates $f(x_n)$ and the output x_{n+1} is sampled onto C_1. On phase ϕ_2 the value of x_{n+1} is transferred to C_2 so that it can subsequently be held constant at the input of the map circuit during the next iteration. Sometimes, the buffer is omitted, and instead a large ratio of C_1/C_2 is used to reduce the charge-sharing error of the second S/H [1].

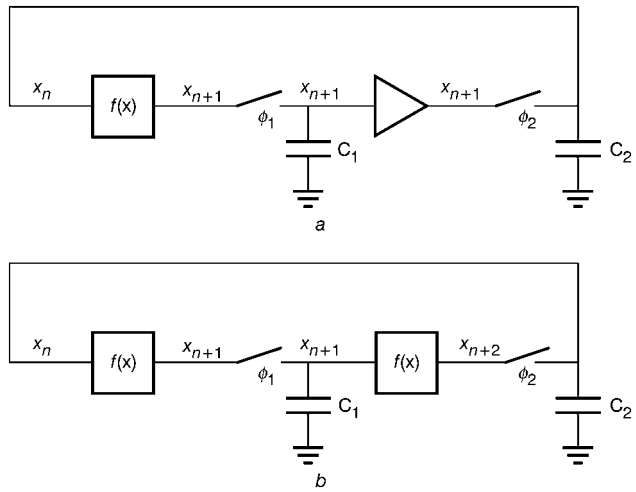

Fig. 3 *Chaos generators*
a Using one map circuit and buffer *b* Using two map circuits

The settling time t_{set} of the map circuit loaded by C_1 sets the limit on the minimum duration of ϕ_1. The time required to perform the second S/H (phase ϕ_2), however, reduces the maximum operating frequency of the chaos generator. We propose here an interesting alternative, shown in Fig. 3*b*, which allows the generation of chaotic samples at the maximum rate of $f_{max} = 1/t_{set}$. In this oscillator two map circuits are used. On phase ϕ_1 the first map circuit generates the output signal which corresponds to $x_{n+1} = f(x_n)$. Then, on phase ϕ_2, the second map circuit generates the output signal which corresponds to $x_{n+2} = f(x_n+1)$. A simple analogue switch could be used to select one of the map circuit outputs on ϕ_1 and the other on ϕ_2, thus maximising the frequency of the generated chaotic samples. Using two map circuits is efficient: all transistors in the oscillator contribute to the essential operation of the map circuit or act as switches and no circuit area or power consumption is wasted on the S/H buffer.

Results: The circuit has been simulated using 0.6 μm CMOS process

parameters. The transistors in the map circuit were sized (W/L) as follows: $M_1 = 4\ \mu m/0.6\ \mu m$, $M_2 = 4\ \mu m/0.6\ \mu m$, $M_3 = 20\ \mu m/0.6\ \mu m$. The power supply was set to $V_{DD} = 5$ V. The switches in the chaos generator were implemented by p-MOS transistors ($W/L = 4\ \mu m/0.6\ \mu m$), while C_1 and C_2 were implemented by the inherent input capacitances of the map circuits so that the chaos generator circuit consists of eight transistors only. It has to be mentioned, that dynamic effects due to charge injection from the switches, use of transistor gate-source capacitances as sample/hold capacitors, etc. somewhat modify the effective map, as compared with the simulated DC transfer characteristics of the map circuit shown in Fig. 2. Nevertheless, in the envisaged applications the actual shape of the map is of no great importance, as long as a chaotic signal is obtained.

The results of transient simulations are shown in Fig. 4. Periodic and aperiodic signals can be observed for different values of V_{BIAS}. Fig. 5 shows a bifurcation diagram, obtained by plotting the values of 5×10^4 output signal samples while sweeping the V_{BIAS} value from 0 to 5 V. Regions of observable chaos, as well as periodic windows, can be clearly seen.

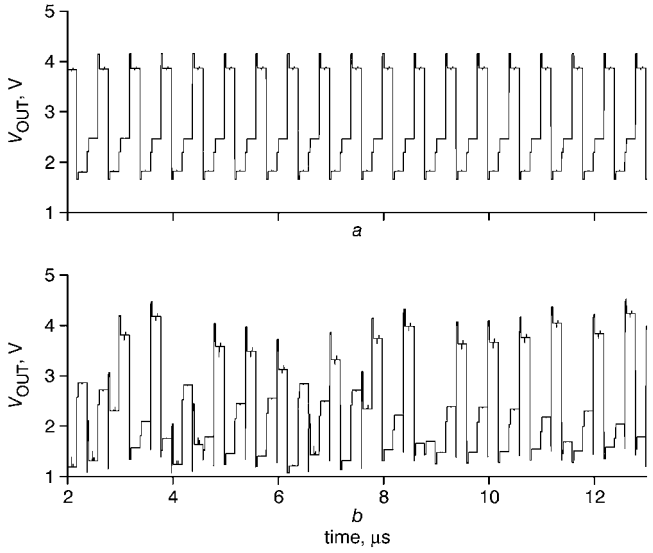

Fig. 4 *Simulated voltages at map circuit output*
a Periodic signal for $V_{BIAS} = 1$ V *b* Chaotic signal for $V_{BIAS} = 2$ V

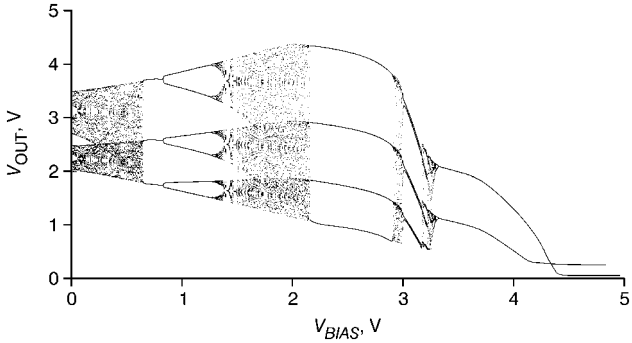

Fig. 5 *Simulated bifurcation diagram of proposed chaos generator*

Conclusion: A new compact chaos generator, based on a three-transistor chaos map circuit, has been proposed. The operation of the circuit has been verified via simulations. Owing to its small size, the circuit is particularly suitable for applications requiring a very large number of uncorrelated random signal sources on a single VLSI chip.

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