An area and power efficient discrete-time chaos generator circuit

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Abstract — **A discrete-time chaos generator circuit suitable for low power applications is presented in this paper. The generator is based on a three-transistor circuit which creates an easily adjustable chaos map characteristic. The circuit has a very compact implementation which makes it suitable for applications where many random noise generators are required on the same chip. The operation of the circuit has been verified via simulations in a 0.6μm CMOS process.**

1. INTRODUCTION

Integrated circuit implementations of non-linear deterministic systems which display chaotic behaviour have been a subject of continuing research during the last decade [1-7]. Discrete-time chaos circuits generate a chaotic series through an iterative application of a suitable non-linear function (chaos map), $f(x)$, as follows:

$$x_{n+1} = f(x_n) \qquad (1)$$

Circuits which generate chaotic signals can be built by using sub-circuits that approximate 'tent', 'logistic', 'Bernoulli shift', or other well-known chaos maps [1, 2]. The chaotic signals generated with these maps have particular properties (for example, chaotic signal generated with the tent map has a flat probability density function of the signal value). In order to construct these maps accurately, the circuits reported in the literature are usually built using a considerable number of transistors and as a consequence are rather large when implemented in custom silicon, and typically consume relatively large amount of power. In certain applications, however, the proprieties of the generated chaotic signals do not need to meet strict statistical or frequency spectrum requirements. Instead, a general random-like, unpredictable signal is required. The exact shape of the chaos map is then of lesser importance than its overall "stretch and fold" characteristic. In [8] we reported a compact chaos generator comprising two V-shape chaotic map circuits. However, even though that circuit occupies a small circuit area when implemented in custom silicon [9], it consumes considerable amount of power. In this paper we present the design of a three-transistor tent-like map circuit, which is efficient in terms of both area as well as power dissipation. The chaos generator based on this map circuit (plus additional switches and a voltage follower circuit) consumes approximately 3.5 μW operating at 50 kHz, with a voltage supply of 3.3 V in a 0.6 μm CMOS technology. The circuit is suitable for use in applications requiring large number of random signal generators on a single chip, such as stochastic neural networks [10].

2. CHAOS GENERATOR

In order to generate the iterative function given by (1), in addition to a nonlinear circuit the discrete-time chaos generator will need two analogue storage locations and a buffer, as illustrated in Fig. 1. The storage is provided by sample-and-hold circuits (switches and capacitors). A two-phase clock signal controls the switches. On phase ϕ_1 the nonlinear circuit computes $y(x_n)$. This is stored on capacitor C_1. On phase ϕ_2 the value $y(x_n)$ is transferred by the buffer, so that x_{n+1} is stored on capacitor C_2. This process continues iteratively. The overall chaos map is determined by the characteristic of the nonlinear circuit, as well as the transfer characteristic of the buffer (typically linear). Second-order effects, associated with the capacitive coupling and sampling operation will also affect the operation of the circuit, but they can be ignored in a first-order analysis.

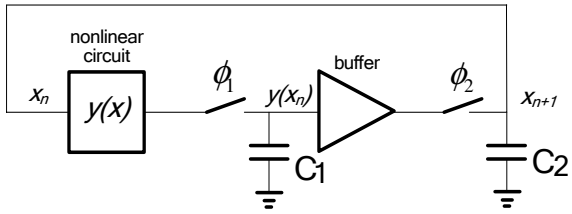

Fig.1. Discrete-time chaos generator circuit

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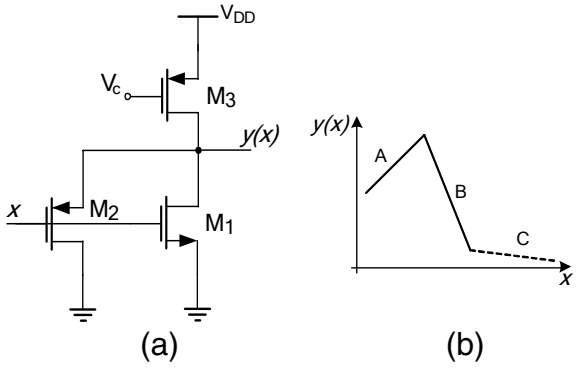

Fig.2. (a) three-transistor map circuit (b) a "tent-like" map transfer characteristic

2.1. Three-transistor map circuit

The three-transistor circuit we propose for generating a suitable chaos map is shown in Fig. 2a. It has been designed to approximate the nonlinear characteristic shown in Fig. 2b. The operation of the circuit can be qualitatively explained as follows.

Assume that the input voltage x is being increased from 0 V. Note that the currents from M_2 and M_1 are summed and flow through M_3. For values of the input voltage x less than the threshold voltage of M_1 the transistor M_1 is switched off. Transistor M_2 is placed in a source follower configuration, with transistor M_3 as a load, producing the positive slope of the DC transfer characteristic (branch A in Fig.2b). As the input voltage x is increased, when x is greater than the threshold voltage of the transistor M_1 this transistor enters saturation region and starts to sink current, forming an 'inverter' with M_3 as a load, thus starting to generate the negative slope of the DC transfer characteristic (branch B in Fig.2b). As x increases and $y(x)$ decreases the transistor M_2 will turn off. Finally, M_1 will enter the triode region (branch C in Fig.2b).

The shape of the characteristic is controlled by changing the biasing current provided by M_3, through changing the control voltage V_C. The transfer characteristic can be thus varied for different values of the control voltage V_C, as illustrated in the circuit simulation result shown in Fig. 3. As a consequence, different values of the control voltage will determine whether the circuit can be used for generating chaotic or periodic signals.

It should also be pointed out that the power dissipation in this circuit is limited by the amount of current that is provided by transistor M_3. This is a major improvement over the circuit we have presented in [8].

2.2. Chaos generator circuit

The complete circuit for generating chaos signal is shown in Fig. 4. The map circuit is made of transistors M_1-M_3, as described above. The switch M_{s3} is used to power down the map circuit when it is not being used (i.e. when ϕ_1='0'), to reduce the overall power dissipation. The buffer is made of transistors M_4 and M_5 in a source follower configuration, with M_{s4} used as a switch for reducing the power dissipation in the buffer (the buffer is powered-down when ϕ_2='0'). In this configuration the storage capacitors (C_1 and C_2 in Fig. 1) will be formed by the input capacitances of the transistors M_1, M_2 and M_4.

During clock phase ϕ_1 (M_{s1} closed) the input of the chaos generator is equal to x_n, the map circuit computes $y(x_n)$ generating x_{n+1} at the output of the buffer. When M_{s1} opens the value of $y(x_n)$ is held on the input capacitance of M_4. While the buffer preserves x_{n+1}, the chaos map can be disconnected from the power supply. Introducing the switch M_{s3}

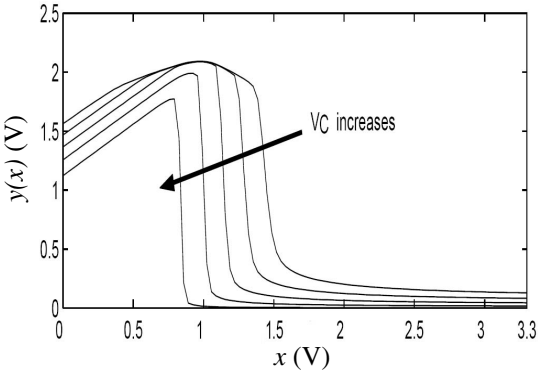

Fig.3. The DC characteristics of the three-transistor map circuit

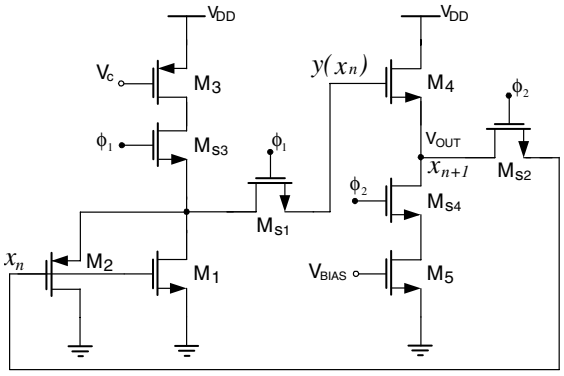

Fig.4. Circuit diagram of the proposed chaos generator

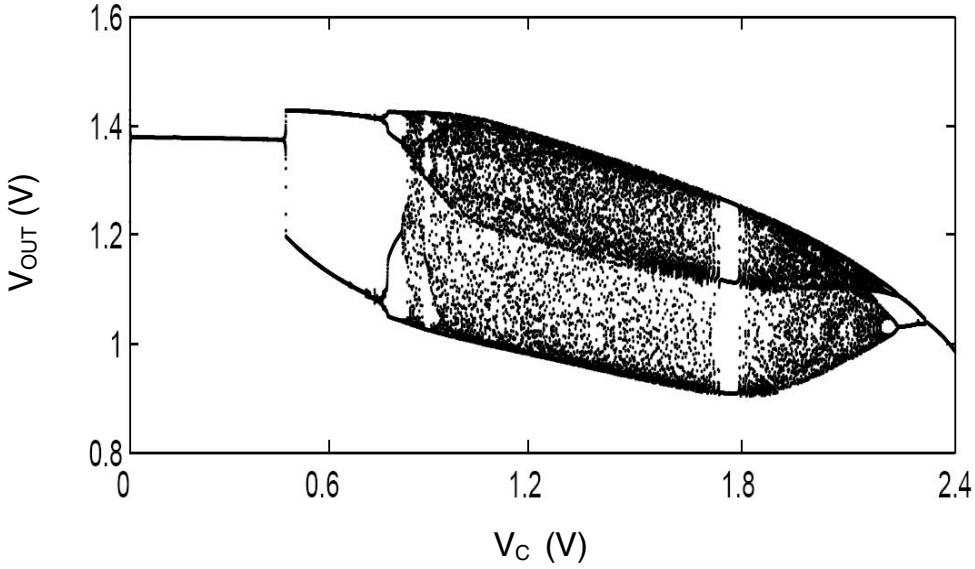

Fig.5. Simulated bifurcation diagram of the proposed chaos generator

and turning it off when the chaos map does not "work" reduces the overall power dissipation. The same can be applied to the follower where the transistor M_{s4} has been introduced (turned on only during phase ϕ_2).

3. SIMULATION RESULS

The circuit was simulated using Spectre, with AMS 0.6μm CMOS process parameters. Transistor sizes used in the map circuit were as follows (W/L values in μm/μm): M_1=1/0.6, M_2=4/0.6, M_3=1/1. These values were also used to generate the characteristic in Fig. 3. Transistors in the buffer were M_4=15/0.6, M_5=1/5. The switches were M_{s1}=M_{s2}=M_{s3}=M_{s4}=2/0.6. The power supply was set to V_{DD} = 3.3 V and V_{BIAS} = 1 V.

The bifurcation diagram of the chaos generator, when the control voltage V_C is swept between 0 V and 2.4 V, is presented in Fig. 5. One can easily observe the chaotic behaviour of the circuit, with periodic windows and regions of observable chaos.

Transient waveforms of the circuit, illustrating the generation of periodic and non-periodic signals for different values of the control voltage V_C are presented in Fig. 6: a chaotic output signal, for V_C = 1.6 V, is depicted in Fig. 6a; a periodic signal, for V_C = 0.6 V, is shown in Fig. 6b.

The minimum pulse duration of the non-overlapping clock phases (ϕ_1 and ϕ_2) for which the outputs of the map circuit and the buffer have enough time to settle is equal to approximately 240 ns. This means that the maximum operating frequency is just above 2 MHz. The circuit will actually generate chaotic signals for higher operating frequencies as well, but its chaotic behaviour at higher frequencies will be modified, since the dynamic effects have to be taken into account as the circuit is no longer performing simple discrete-time iteration of the chaos map (values are sampled before they settle).

In some applications, however, random signal samples are required at a lower rate. The proposed chaos generator circuit optimises power consumption at lower operating frequencies. If the clock pulse duration is kept constant, at 240 ns (i.e. switches M_{S1}, M_{S2}, M_{S3} and M_{S4} are on for 240 ns only within each clock period) and the frequency is decreased then the overall power consumption of the circuit decreases. In Fig. 7 the power consumption versus the frequency of operation is shown; here the pulse width was kept constant (240 ns) for all the frequencies depicted, and the control voltage had the value of V_C = 1.6 V.

4. CONCLUSIONS

A new area and power efficient chaos generator has been proposed. The properties of the generated signals were of no critical importance in this work as long as a random-valued signal was produced. Simulation results indicate that the proposed circuit can be used to generate chaotic signals, as well as periodic signals, for various values of a single control parameter (voltage V_C). The circuit will occupy small area in a

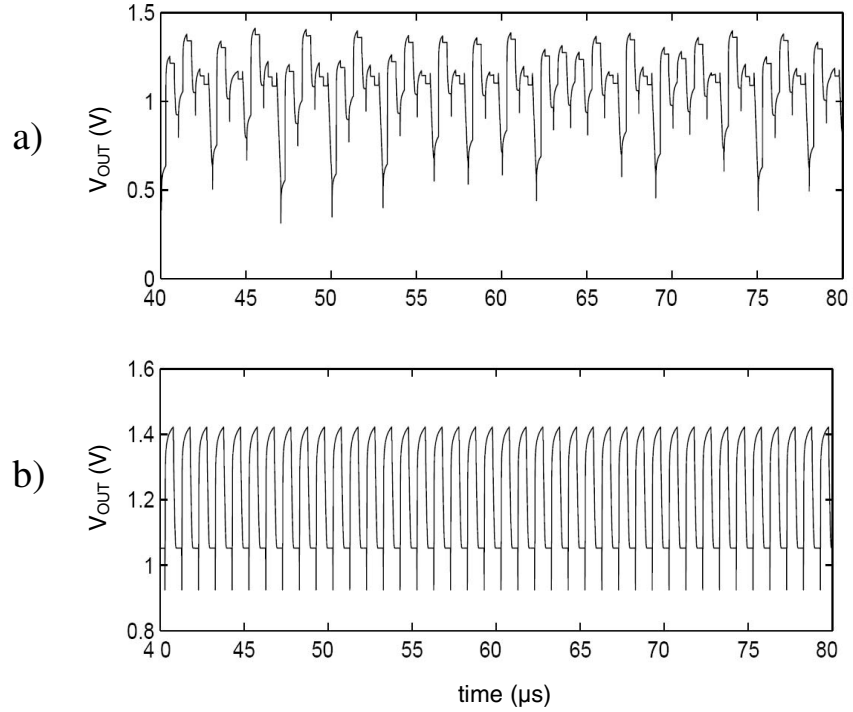

Fig.6. Simulated voltages at the map circuit output; (a) chaotic signal for $V_C = 1.6$ V; (b) periodic signal for $V_C = 0.6$V.

custom silicon implementation, and the power consumption of the proposed circuit is low, it is therefore very suitable for applications where a large number of uncorrelated random signal sources are required on a single chip.

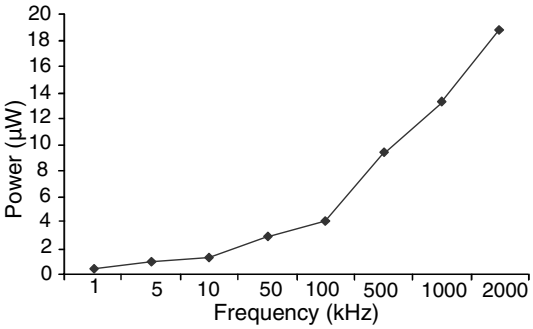

Fig.7. Power consumption of the chaos generator as a function of operating frequency

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