Vision Sensor with a SIMD Processor Array in a Vertically Stacked 3D Integrated Circuit Technology

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***Abstract*—We present a design of a vision sensor device, implemented in a three-dimensional (3D) silicon on insulator (SOI) 150nm CMOS technology. The proof-of-concept device contains an image sensor array on one layer, and a pitch-matched array of 32x32 pixel-parallel processors, distributed over two further layers. The processor array uses mixed-mode processing elements and operates in SIMD (Single Instruction Multiple Data) mode, providing low-level image processing operations on the sensory data. The inter-layer communication is achieved by means of through-silicon vias (TSVs), on a pixel-parallel level, and the system is partitioned to minimise the area overhead associated with this communication.**

I. INTRODUCTION

The basic concept of a 'vision chip' is illustrated in Figure 1. Unlike a conventional computer vision system, which separates image acquisition and image processing, the vision chip performs processing adjacent to the sensors, on the same device, producing as outputs pre-processed images, or even higher-level information such as lists of features, presence and locations of specific objects, or other information extracted from the visual scene. The advantages of this approach include the removal of the sensor/processor bottleneck, and associated reduction in power consumption and increase in the processing throughput. In the past, we have developed a number of devices [1-3] based on a pixel-per-processor architecture, where a massively parallel processor array is integrated with the image sensor array, which provides pixel-parallel input to the array. We have considered analogue and digital processor implementations. Here we present the design of a mixed-mode processor array [4], integrated with image sensors in a 3-layer 3D silicon technology.

When processing circuits are placed next to sensors in a standard planar technology, the fill-factor is very significantly reduced, leading to lower sensitivity of the device. The achievable pixel pitch is also severely constrained. Vertically integrated 3D silicon technology, with fully random-placed through silicon vias (TSV) [5], offers unique advantages that solve most of these problems. A sensor array, with optimized noise and sensitivity, can be placed on top of CMOS processing circuitry. Furthermore, processing circuitry can be distributed across several layers, maintaining the pitch of the sensor array, for a fully pixel-parallel processor array at high resolution.

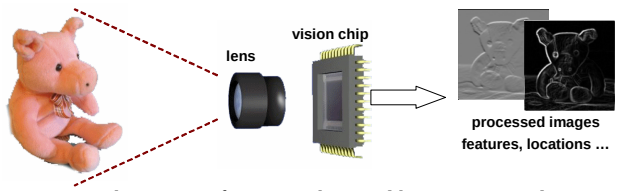

Figure 1. The concept of a 'vision chip'. Unlike a conventional image sensor, it outputs information extracted from the images.

II. SYSTEM ARCHITECTURE

The outline of the proposed system is shown in Figure 2. Three silicon tiers contain sensing, analogue and digital processing layers, which form an integrated cellular sensor/processor array. The processing element (PE) cells span across three layers, and are arranged on a regular 2D grid, with 4-nearest-neighbour connections. The images are acquired in the photosensing layer, and processed in the pixel-parallel SIMD (Single Instruction Multiple Data) processor array, according to a program that is broadcast to all PEs from a single controller (currently implemented off-chip). No A/D conversion is necessary for gray-level processing, as the Analogue Processing Element (APE) part of the PE operates directly on the analogue pixel data. The current-mode photosensors provide currents corresponding to the incident light. These currents are then processed using switched-current circuits, operating as a datapath of a simple software-programmable processor [2]. After segmentation or other feature/object extraction operation is performed, additional processing steps can be carried out on binary images, which is performed in the Digital Processing Element (DPE) part of the PE. The DPE and APE can interact and the results of logic operations in the DPE can modify the subsequent gray-level processing steps. In the SIMD array, all PEs perform the same instruction on their respective data, but some degree of autonomy is achieved through the use of activity flags, which

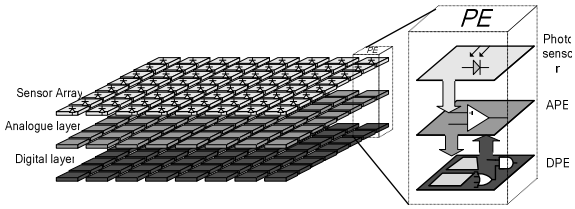

Figure 2. Architecture of the proposed 3D vision chip. Sensing/ processing elements (PEs) are physically distributed across 3 layers.

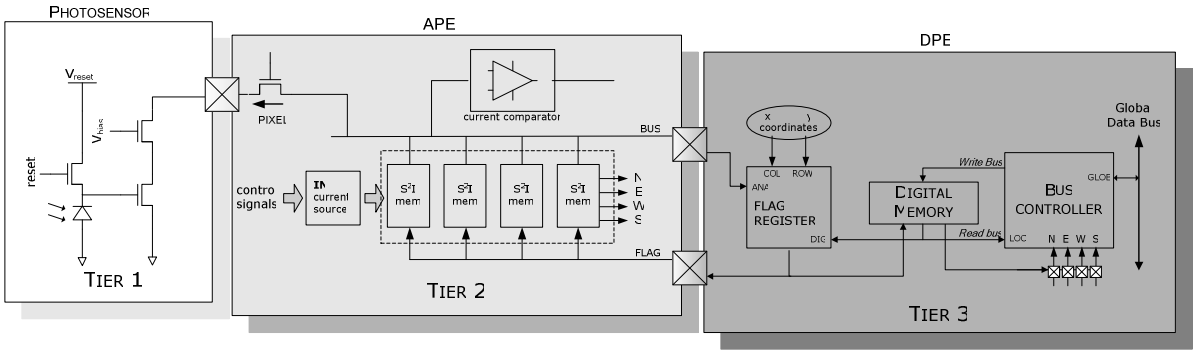

Figure 3. Processor/pixel design. The PE comprises a current-mode photosensor, Analogue Processing Element (APE) and Digital Processing Element (DPE).

locally enable/disable individual PEs in the array. Such conditional branching can be made upon the result of a gray-level operation (via comparator in the APE) or the result of a logic operation (in the DPE).

III. IMPLEMENTATION

The designed array is a small-scale proof-of-concept device, containing 32×32 pixel-processors with a 30μm pitch. It uses 3-layer MITLL 150nm SOI CMOS technology. The chip has been taped-out, but fabricated samples are not yet available. The figures reported below are based on simulations.

The schematic diagram of the PE is shown in Figure 3. Photosensors will be backside illuminated. Three different sensor designs (including a photogate-based design) have been used in different parts of the array. They work in integration mode, with cascode-based current readout. The APE consists of four analogue current-mode memory cells, local (4-neighbour) and global I/O, and a comparator circuit, connected to a common analogue bus through switches. The operation follows the general principles of instruction-level programmable analogue processing [2]. The memory cell uses a modified S^2I circuit. It operates with a 2.5uA reference current and 1.5V supply voltage. The DPE contains 12 bits of local SRAM, flag register and a bus controller (BC). It is capable of executing the full set of Boolean operators and asynchronous binary wave-propagations for fast geodesic reconstruction and similar operations [4].

To minimise the overhead associated with the TSVs, the system has been partitioned into sensing, analogue and digital processing layers, laid out on separate tiers, and the communication between the APE and the DPE has been achieved using a minimum number of two TSVs. The binary comparison result is passed from the APE to the DPE while the binary local activity flag value is passed from the DPE to the APE. This communication allows effective execution of both gray-scale and binary operations on the pixel data. The APE receives input from the sensor layer through a single TSV. Control signals for all the layers are distributed on the respective layers, and the overall coordination of activity and communication is ensured through the synchronised control of all layers. The array supports random read-out of digital or analogue values.

The APE circuitry contains 56 transistors (mostly larger than minimum-size, to minimise data processing errors caused by mismatch), and DPE circuitry consists of 157 transistors (mostly minimum-size). Based on post-layout simulations, The DPEs are expected to operate at 350 MHz, providing 179×10^9 binary operations per second. The asynchronous processing unit will provide further performance gain. Analogue (gray-level) operations were designed to be executed at 10 MHz rate, with signal-dependent error below 1% and error matching (main contribution to fixed-pattern noise of gray-level processing) better than 0.1%.

IV. CONCLUSIONS

We have designed pixel-parallel SIMD sensor/processor array vision chip in a 3D vertically integrated technology. Analogue and digital processing circuits provide optimised performance for specific tasks. The analogue processors have superior efficiency when performing gray-scale operations with moderate accuracy, while digital processors offer increased robustness to noise, higher speed, and more compact design for binary operations, long-term storage, and high-precision computations. In the present design, all layers are implemented using wafers fabricated in the same technology, but it can be easily seen that heterogenous integration of various process technologies, enabled by the vertical integration, will further improve the performance of each layer. Furthermore, extending the design to a greater number of layers will enable further improvements in the functionality, performance and local memory capacity of the processing elements. The pixel-parallel processor arrays appear an exceptionally suitable architecture for 3D integration, providing good scalability to a greater number of layers.

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