Characterization of processing errors on analog fully-programmable cellular sensor-processor arrays

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***Abstract*— Analog processor arrays, particularly for vision chips, have been in development for a number of years. Based normally on the SIMD computing paradigm, they achieve very high instruction parallelism through use of compact processing elements. A fundamental aspect of processor operation is the ability to copy content of a register to another. This operation carries with it a number of errors. This paper identifies these errors and provides the means by which they can be separated and measured. These techniques can then be applied to analyze any operation upon an analog processor array. The results from such an analysis reflect on the susceptibility of the circuit to process mismatch, and thermal and switch noise performance of a particular analog memory design.**

I. INTRODUCTION

Analog processor arrays have been in development for inclusion in vision sensors or image processors for a number of years [1,2]. For lower cost process nodes (e.g. 180nm) they have offered simple integration with light sensors and higher functionality per unit area than is feasible by a digital counterpart in the same process node. Additionally, they have shown high power efficiency and speed [2,3,4,5]. The particular processors that we are concerned with in this paper are discrete-time analog processor arrays usually programmed as SIMD computers (Fig.1). These processors are fed instructions, which they execute in a similar clocked manner as digital processors, with typical operational frequencies of between 1MHz and 10MHz.

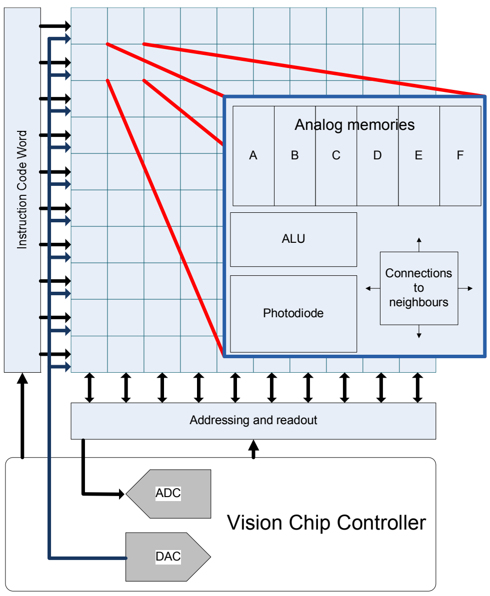

Figure 1. Schematic of a generic cellular processor array with external controller.

While characterization of digital processors is relatively straightforward, analog processing brings with it a spectrum of metrics generally unknown to the digital programmer. Analog processors will always produce an erroneous result to some degree. In this paper, we provide a framework for the characterization of these errors. Through an understanding of the operational attributes of analog processors, we may realize workarounds, choose different algorithms or indeed output the data and process off-chip.

Storage elements commonly used within analog processor arrays are usually switched-current [6] or switched capacitor cells [7], each of which has advantages dependent on the desired computation, SC cells being ideally suited to signal averaging, such as performing diffusion operations with SI cells suited to addition, subtraction operations.

II. ERROR MODEL AND CHARACTERIZATION

The particular operation we characterize in this work is that of "copy". This then can provide a model by which other operations may be characterized. The effect of the copy operation within an SIMD array computer is to replicate a register's contents within every processor element, i.e. for an M x N array of elements:

$$A_{i,j} = B_{i,j} \tag{1}$$

where $1 \leq i \leq M$ and $1 \leq j \leq N$. The operation considered in shorthand is simply A ← B. Generally a means is provided for setting a register with a code *c*. Through this system, it is possible to set an initial register **B** to any value within its dynamic range. Both initial register **B** and target register **A** may then be readout.

The copy process is accompanied by an error ($E_{i,j}$) specific to each and every processor element; it is this error that we wish to illuminate. $E_{i,j}$ is the difference between the internal stored values $A_{i,j}$, and $B_{i,j}$ and is a function of time, *t* and *c*, the code (or signal level) with which the source register (**B**) is initially loaded. The error can be decomposed into an offset of $E_0(c) + \delta_{i,j}(c)$, where $E_0(c)$ is the array mean offset and $\delta_{i,j}(c)$ is a PE specific or fixed pattern offset around the mean, and a time dependent offset for each transfer of $\varepsilon_{i,j}$. For a single transfer, the error is given by:

$$A_{i,j}(c,t) - B_{i,j}(c,t) = E_{i,j}(c,t) = E_0(c) + \delta_{i,j}(c) + \varepsilon_{i,j}(c,t) \tag{2}$$

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If the internal transfer is repeated R times, with repeats numbered $1 \leq r \leq R$ then

$$E_{i,j}(c,R,t) = R\big(E_0(c) + \delta_{i,j}(c)\big) + \sum_{r=1}^{R} \varepsilon_{i,j}(c,t_r) \quad (3)$$

Equation (3) shows the correlated noise of the offset increasing by a factor of R. Random noise (ε) is uncorrelated and is assumed white gaussian in nature; thus (right-hand-side of (3))

$$\sum_{r=1}^{R} \varepsilon_{i,j}(c,t_r) = \sqrt{R}\varepsilon_{i,j}(c,t) \quad (4)$$

When array memories **A** and **B** are read-out (equivalent to reading out two frames), additional noise is added constituting a read-out noise N_A and N_B for each frame, with additionally a fixed pattern noise (FPN), F for the second frame (**A**). While normally inconsequential, this FPN arises from the finite degradation that has occurred to register **A** during the course of register **B**'s readout; this is caused by register **A**'s extended storage time (relative to **B)** and readout switching effects. If the entire repeat copy process is repeated Q times (in sequence where $1 \leq q \leq Q$) then the difference between two observable frame measurands (for **A** and **B**) for the q'th frame-pair is:

$$\Delta_{i,j}(c,R,t_q) = A'_{i,j}(c,R,t_q) - B'_{i,j}(c,t_q) \quad (5)$$

with the relations between read-out (A' and B') and internal values being:

$$A'_{i,j}(c,R,t_q) = A_{i,j}(c,R,t) + N_A(t_q) + F_{i,j}(c) \quad (6)$$

$$B'_{i,j}(c,t_q) = B_{i,j}(c,t) + N_B(t_q) \quad (7)$$

From (2,5-7):

$$\Delta_{i,j}(c,R,t_q) = E_{i,j}(c,R,t_q) + N_A(t_q) - N_B(t_q) + F_{i,j}(c) \quad (8)$$

By careful processing of the read signals ($\Delta_{i,j}$) each individual error source (within $E_{i,j}$) can be extracted. We start the process with determining the scalar average offset error $E_0(C)$.

A. Average offset error

If the Q frame-pairs are averaged (denoted by overbars); this reduces the magnitude of the temporal noise sources by a factor of $\sqrt{Q}$. Taking the pixel-wise array average of Q frame-pairs of (8) with substitution from (3-4) gives us:

$$\overline{\Delta_{i,j}(c,R,t)} = \overline{R\big(E_0(c) + \delta_{i,j}(c)\big)} + \overline{F_{i,j}(c)} + \frac{\overline{\sqrt{R}\varepsilon_{i,j}(c,t) - N_B(t) + N_A(t)}}{\sqrt{Q}} \quad (9)$$

Once the array average of (9) is taken, the uncorrelated noise terms (ε, N_A, N_B) become (even more) insignificant and since the mean of array FPN (δ) is by definition zero, the sampled array average of read-out error differences is:

$$\overline{\Delta(c,R)} = \frac{\sum_{j=1}^{N}\sum_{i=1}^{M}\left[\overline{\Delta_{i,j}(c,R,t)}\right]}{NM} = R\,E_0(c) + F(c) \quad (10)$$

Taking two data-sets with R copy operations and $R=1$, allows $F(c)$ to be removed to determine $E_0(c)$:

$$E_0(c) = \frac{\overline{\Delta(c,R)} - \overline{\Delta(c,1)}}{R-1} \quad (11)$$

The deviation around this error, across the array, is the FPN (δ) which we now determine.

B. Fixed pattern noise

The FPN of a register copy is the standard deviation of the offset error. Using the principles of propagation of error[8], and assuming that $\overline{N_A(t_q)} = \overline{N_B(t_q)}$ and that they are uncorrelated, the variance (σ^2) of the pixel difference of the two frames at read-out is

$$\sigma^2_{\Delta(c,R)} = \left(\frac{\partial \delta_{i,j}}{\partial t}\right)^2 \sigma^2_{\delta(c)} + \left(\frac{\partial F_{i,j}}{\partial t}\right)^2 \sigma^2_{F(c)} + \left(\frac{\partial \varepsilon_{i,j}}{\partial t}\right)^2 \sigma^2_{\varepsilon(c)} + \left(\frac{\partial \varepsilon_{i,j}}{\partial t}\right)^2 \sigma^2_{N_A} \quad (12)$$

Applying this principle to (9) over all pixels (all i,j), the variance of frame error is:

$$\sigma^2_{\Delta(c,R)} = R^2\sigma^2_{\delta(c)} + \sigma^2_{F(c)} + \frac{R}{Q}\sigma^2_{\varepsilon(c)} + \frac{2}{Q}\sigma^2_{N_A} \quad (13)$$

With typical values of $R = 5$ and $Q = 20$, it is usually unnecessary to consider the last two terms of this equation; this can be confirmed by later calculation of random and readout errors.

From (13), the code-dependent standard deviation of offset (i.e. fixed pattern noise) of register copy can be found:

$$\sigma_{\delta(c)} = \sqrt{\frac{\sigma^2_{\Delta(c,R)} - \sigma^2_{\Delta(c,1)}}{R^2-1}} \quad (14)$$

with:

$$\sigma^2_{\Delta(c,R)} = \frac{\sum_{j=1}^{N}\sum_{i=1}^{M}\left[\overline{\Delta_{i,j}(c,R,t)} - \overline{\Delta(c,R)}\right]^2}{NM} \quad (15)$$

Equation (15) provides an array-global fixed pattern noise metric for register copy. It can be useful to view the FPN graphically in addition. By a similar derivation from (9), each pixel's offset is given by:

$$\delta_{i,j}(c) = \frac{\overline{\Delta_{i,j}(c,R,t)} - \overline{\Delta_{i,j}(c,1,t)}}{R-1} - E_0(c) \quad (16)$$

Many image processing algorithms are based on spatially localised operations (e.g. convolution kernels etc). In many such cases, global low-frequency spatial variation that contributes to the FPN calculated across the entire array is much less of a problem (especially if local average can be easily obtained and compensated for). However variation seen in a 'local' zone is not correctable, hence it is useful to determine a figure for local FPN. Taking a 5x5 grid of pixels, the local variance is defined as:

$$\sigma^2_{\Delta Loc_{u,v}(c,R)} = \sum_{j=1}^{5}\sum_{i=1}^{5}\frac{\left(\overline{\Delta_{u+i,v+j}(c,R,t)} - E_{u,v}(c)\right)^2}{25} \quad (17)$$

with local average $E_{u,v}(c)$ given by:

$$E_{u,v}(c) = \sum_{j=1}^{5}\sum_{i=1}^{5}\frac{\left(\overline{\Delta_{u+i,v+j}(c,R,t)}\right)^2}{25} \quad (18)$$

To afford a single measure of the local FPN, the array average of the local FPN figures is taken:

$$\sigma^2_{\Delta LocAvg(c,R)} = \sum_{u=1}^{N-4}\sum_{v=1}^{M-4}\frac{\sigma^2_{\Delta Loc_{u,v}(c,R)}}{(N-4)(M-4)} \quad (19)$$

C. Random Noise

If PEs are considered as individual entities, then errors relative to other pixel's of the array can be excluded (i.e. E_0, δ and F); a PEs output error will vary only with those variables that are time dependent, i.e.N_A, N_B and random noise of register copy, ε, which we determine in this section. Applying error propagation to a single pixel's differences

$(\Delta_{i,j})$ in the same manner as in (12), and without the benefit of averaging Q samples, yields a function of its variance:

$$\sigma^2_{\Delta_{i,j}(C,R)} = R\sigma^2_{\varepsilon_{i,j}(C)} + 2\sigma^2_{N_A} \tag{20}$$

The variance of a pixel's error at read-out is determinable from measurements and is given by:

$$\sigma^2_{\Delta_{i,j}(C,R)} = \frac{\sum_{q=1}^{Q}\left[\Delta_{i,j}(c,R,t_q)-\overline{\Delta_{i,j}(c,R)}\right]^2}{Q} \tag{21}$$

with mean $\overline{\Delta_{i,j}(c,R)}$ given by the average of Q samples:

$$\overline{\Delta_{i,j}(c,R)} = \frac{\sum_{q=1}^{Q}\Delta_{i,j}(c,R,t_q)}{Q} \tag{22}$$

Determining random noise for copy per pixel $(\sigma_{\varepsilon(c)})$ is then feasible, but since there is only a small increase in noise due to increased repeats (relative to the magnitude of readout noise), improved results are obtained by assuming that random noise of register copy is equal across the array. In this case, the array average of the variance of read-out error can be determined:

$$\sigma_{\Delta\_AVG(c,R)} = \sum_{j=1}^{N}\sum_{i=1}^{M}\frac{\sigma^2_{\Delta_{i,j}(C,R)}}{NM} \tag{23}$$

From (20) and by taking two parallel data sets with *R=1* and *R* copies, we can then find the random error of register copy for the average pixel:

$$\sigma_{\varepsilon(c)} = \sqrt{\frac{\sigma^2_{\Delta\_AVG(c,R)}-\sigma^2_{\Delta\_AVG(c,1)}}{R-1}} \tag{24}$$

If necessary, this data can be fed back into equation (13) to improve the accuracy of the determination of $\sigma_{\delta(C)}$; however, this is not normally necessary.

III. Results

Two different analog processor arrays were acquired, programmed and tested at room temperature; we will refer to these systems as System α and System β. We do not identify the systems since our intention in this work is to advocate the testing methods used rather than promote a particular system's merits/demerits.

The measurement process used 20 repeats of each measurement (i.e. *Q=20*) with the number of internal copy repeats (*R*) taking values of 1,2,3,4,5 and 6. Codes of 0 to 255 in approximate steps of 16 were input to the devices (17 values). With two frames per measurement, a total of 4080 frames were available for processing from each system.

The pseudo-code for this acquisition is:

```
for c = 0 to 255 step 16 [last step increments 15]
  for q =1 to Q
    load X, #c
    OUTPUT X          [Frame B]
    for r = 1 to R
      Y ← X
      X ← Y
    next r
    OUTPUT X          [Frame A]
  next q
next c
```

Note that for the purposes of this work, a single copy iteration is composed of two transfers in order to facilitate the repeat process. During the analysis. these are treated as a single transfer. For uncorrelated random noise, individual transfers will be $1/\sqrt{2}$ of the noise values recorded. For FPN, the net effect of the two transfers is reported; additional work is required if the effect of single transfers is to be determined assuredly.

Shown in Figures 2 and 3 are the four measurements of offset (11), global fixed pattern noise (14), local fixed pattern noise (19) and random noise (24) of register copy for System α and System β respectively (applicable equation in brackets). All measurements are taken for R=6 (and hence make use of the dataset for R=1 in addition).

Figure 4 shows an example of a full data-set for different R values for offset error for System β (from equation (11)). This shows a clear gain error of copy in System β leading to a significant change in code *c* during the course of the multiple copy operation - hence the x-axis points used for this plot (and in addition Figures 2 and 3) is the average of the input and output codes. The fact that the plots lie in the same location for multiple measurements taken with different values of R indicates the model for this system is correct - indicating the importance of collecting data for multiple values of copy repeat. We have found this an invaluable tool when debugging the measurements and models. Other specific aspects of the data are outlined below.

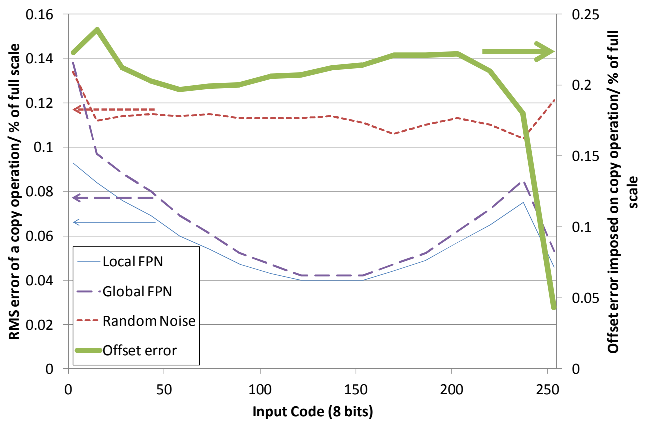

Figure 2. Offset, global FPN, local FPN and random noise of register transfer for System α

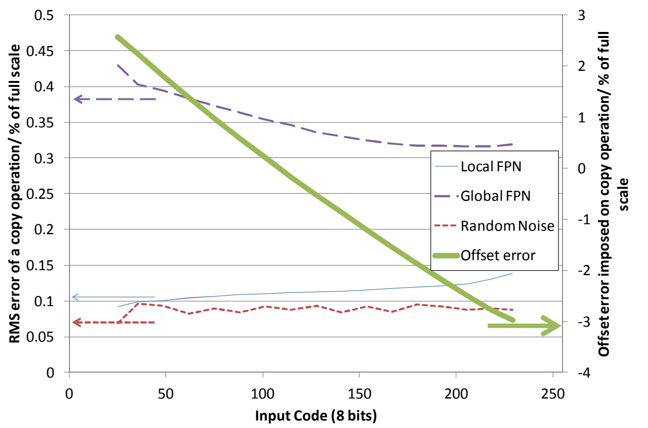

Figure 3. Offset, global FPN, local FPN and random noise of register transfer for System β

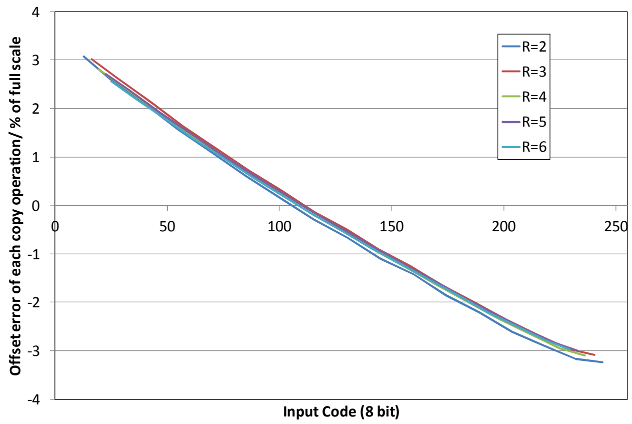

Figure 4. Offset error for each register transfer for System β for different numbers of repeat copies. (Overlapping lines indicate the error model is satisfactory)

A. *Offset Error ($E_0(c)$)*

The average (over all PEs) offset error incurred by a copy operation is shown in the figures. They show a code dependent offset range of 0.25% of full-scale for System α and 7% offset range for System β . However, it is clear from the System β data (Figure 3) that the offset error primarily relates to a gain error in the transfer process.

B. *Fixed pattern noise of register transfer*

The application of significant gain during copy by System β highlighted a need to modify the noise model: FPN generation and temporal noise coupled to the system during early repeat copies gets attenuated by the application of gain in later copies (first two terms of (12)). For example, for 5 copy operations the sum of the FPN noise in (13) needs modifying from $25\sigma_{\delta(c)}^2$ to:

$$\left(\sigma_{\delta(c)} + G\sigma_{\delta(c)} + G^2\sigma_{\delta(c)} + G^3\sigma_{\delta(c)} + G^4\sigma_{\delta(c)}\right)^2 \quad (25)$$

This is simply a change in the effective *R*. Data in Figures 2 and 3 uses this modification with G=0.93 (extracted from Figure 4), i.e. (15) becomes:

$$\sigma_{\delta\_adj(c)} = \sqrt{\frac{\sigma_{\Delta(c,R)}^2 - \sigma_{\Delta(c,1)}^2}{\left(\sum_{y=1}^{R} G^{y-1}\right)^2 - 1}} \quad (26)$$

The data shows FPN to be <0.13% (System α) and <0.46% (System β) for the two systems.

C. *Local Fixed Pattern Noise*

The two systems show much closer matching of local FPN noise figures: 0.09% and 0.17% RMS of full scale for System α and System β, relative to their respective global figures; the local FPN for System β imposed by register transfer is different in character from the global noise figure, indicating that local transistor matching is generally good.

D. *Random Noise of a copy operation*

System α has error of 0.12% RMS of full-scale with System β showing 0.085% RMS error. These errors are generally irrespective of code for both systems. While random noise is less effected by gain error, the same modification is applied to R (i.e. replacement with $\sum_{y=1}^{R} G^{y-1}$) for determining this metric.

IV. Discussion

The absolute offset error introduced by analog memory storage systems is less important than the range of the offset error variation with stored value; a fixed value of offset error may be compensated for by adding a small constant value with every operation. The range of offset error for the two systems is 0.25% and 7% of full-scale range respectively for System α and System β.

The data for random error and fixed pattern error for the two vision chips varies less widely. For System β, the local fixed pattern noise drops to 0.17% relative to the global figure of 0.46%, perhaps indicating the intrinsic matching between PEs is generally good, with a higher, array-wide FPN arising from other issues.

V. Conclusion

The thorough analysis of noise sources within analog processor arrays can reveal specific areas that could lead to performance improvements of future devices. Within a device, local FPN will reflect relative transistor matching, with global effects perhaps relating to power supply fluctuations or instruction timing inconsistencies at different points across the array. Random noise of PE operations has potential to be associated with a number of sources such as that associated with switching or thermal noise of transistor elements. Finally, the extraction of average offset error from other effects caused by readout indicates the efficacy of the register design itself.

VI. Acknowledgement

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