

Demonstration of a Low Power Image Processing System using a SCAMP3 Vision Chip

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Abstract — A low power vision system has been developed incorporating the SCAMP3 pixel-parallel processor array vision chip. A test algorithm to detect loitering targets has shown an average power consumption of <6mW analysing 128x128 images at 8 frames per second.

I. INTRODUCTION

A conventional image processing system incorporates an imaging array, a data acquisition system, microprocessor and large memory. Due to a constant flow of information from the sensor and acquisition system, the attached microprocessor requires a large throughput and processing capability. Such a system is generally not conducive to operating an image processing algorithm at low power levels, and lowering of the frame rate, or reducing the image resolution are usually required in order to meet the power constraints of distributed smart camera nodes [1].

Incorporating an integrated sensor/processor (i.e. a vision chip) in the image processing architecture, allows the system to be re-structured to introduce near-sensor parallel processing, reduce analogue to digital conversions, bandwidth requirements and hence power consumption. A vision chip allows images to be pre-processed on the focal plane, regions of interest labelled and salient information flagged for transfer to a microprocessor.

Vision chips have been in development for a number of years, generally based on the SIMD processor array archetype [2-5]. Such chips consist of a large number of processor elements (PEs) that process data in a pixel-parallel manner. These PEs variously combine digital and analogue processing capability, memories and a photo-sensor. With the addition of global I/O and neighbour communication, powerful pre-processing of data on-chip can be performed.

The SCAMP3 [5] IC (as shown in Figure 1) is an example of such a vision chip, designed with particular attention to low-power operation. It incorporates an array of 128x128 pixels, tightly coupled with elementary processors comprising 9 analogue registers, a flag register (upon which in-cell conditional execution is possible) and neighbourhood communication. It is capable of analogue addition, subtraction and comparison. This vision chip has been operated with many different algorithms (e.g. [5,6]) demonstrating adaptive sensing, motion detection, edge enhancement, segmentation, object sizing etc. Measurements of the vision chip itself (immersed in the vision system) have shown the peak performance of 20 GOPS at 240mW. Importantly, the IC

shows sub-mW power consumption when in a quiescent state. Notably, SCAMP3 does not integrate the traditional functionality of a microprocessor – a program counter, command sequencer etc. Hence, the IC must be incorporated into a wider system incorporating external devices. The external system then allows data capture from the IC, analogue input to the IC, loops and conditional executions to be performed. In this paper, we describe a complete low-power smart camera system based on the SCAMP3 device.

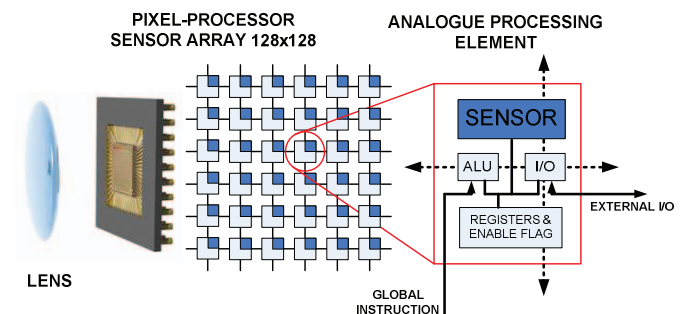


Figure 1. SCAMP3 focal plane processor

II. IMPLEMENTATION

The basic architecture of the low power system is shown in Figure 2.

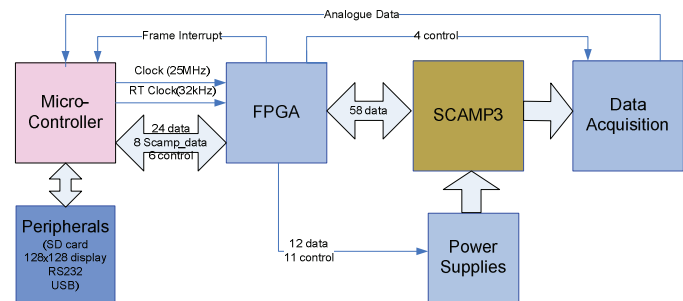


Figure 2. Structure of low power SCAMP3 vision system

The operating regime for the system is depicted in Figure 3. Image pre-processing is carried out by the pixel-parallel processor array on the SCAMP3 chip. The high computational throughput of the device ensures that the computations complete in a very short time; dependant on the algorithm, this is typically between hundreds of μ s to several ms. Readout is only performed when the result of the running algorithm indicates it is required, and typically only global measures

extracted from images are output for further processing, rather than image data. The microcontroller then operates on a much reduced data set. The default operating scenario involves a long down time during which the system is quiescent, apart from the passive integration of light upon the photosensor. The system design aims to exploit this period by entering a low power mode during this time.

The FPGA (Actel AGL400) was selected on the requirement for a large number of outputs and low current consumption in the quiescent state. This allows the FPGA to be used as a real-time clock counter and to perform peripheral functions even when the microcontroller is asleep. The microcontroller used is an NXP LPC1769 device. This incorporates an ARM Cortex M3 core and a range of peripherals including an analogue to digital converter. The device features many different power down modes, with particularly “deep sleep” mode being exploited for this project, whereby the device draws $240\mu\text{A}$. The LPC1769 can operate at 120MHz, but for low power operation we prefer to clock at 25MHz at which frequency the device can operate without the PLL (and its power hungry startup time).

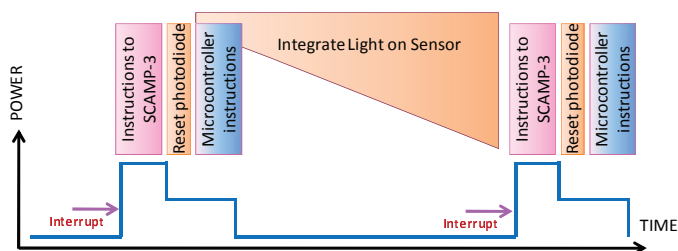


Figure 3. Power use with different operating regimes. Microcontroller instructions are dependant on the result of array processing on SCAMP3

A SCAMP3 system also requires a number of different power supply voltages and biases. Seven fixed voltages are generated by TPS780 (Texas Instruments) linear regulators, with an additional 14 biases generated from a pair of AD5348 ICs (Analog Devices). Linear regulators were preferred in order to avoid noise coupling issues, reduce PCB space and keep quiescent current low. The vision chip also requires an analogue input to globally define a value to all cells. This is provided by an AD5445 driving an OPA355 (TI) op-amp. In order to amplify the current output from the IC, 3 additional op-amps are also required, with current switched between different gains by means of a pair of ADG719 switches.

The system, consisting of two PCBs, with three 1Ah AAA batteries, fits in an enclosure of dimensions 65x50x40mm. The two assembled circuit boards are shown in Figure 4. A number of peripherals can optionally be added to the system including a USB 2.0 link module, an SD card and a 128x128 LCD display.

III. SOFTWARE

The vision system can be operated in two modes. In “algorithm development” mode (using the APRON environment [7]), the system is connected to a USB 2.0 link. In this mode, the precise flow of data on registers on the

SCAMP3 IC can be monitored in real-time. This is a powerful development tool that allows algorithms to be developed swiftly in a high level programming language. It provides the user with visible feedback on algorithm flow allowing intuitive debugging with short time-spans (<5s) between re-compilations.

Once the algorithm has been developed, the low power mode can be enabled. Debugging is still feasible with the externally attached 128x128 display at this stage, but once this has been concluded, the system can then operate in its lowest power mode without external diagnostics.

The different software modes will be demonstrated at the conference.

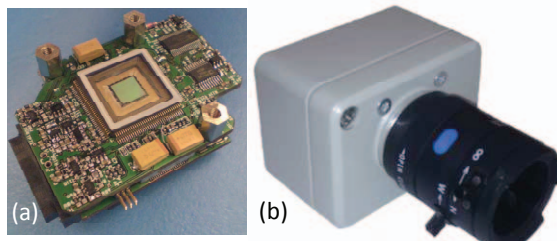


Figure 4(a) System printed circuit boards (FPGA and microcontroller are not visible) (b) full enclosed system

IV. RESULTS AND CONCLUSIONS

In a test algorithm that performed loiterer detection, the vision system was operated analysing 128x128 pixel video at 8fps drawing currents of 0.78mA in sleep and an average of 47mA in operation. The respective times in these modes was 123ms and 2ms, giving an average current draw of 1.5mA. The nominal potential from the batteries was 3.6V giving a power consumption of approximately 5.5mW. The on-time of 2ms is currently the shortest live-time that is feasible due to limitations on the time required for power supplies and voltages to settle, coupled with the start-up time for the 25MHz crystal oscillator. The power consumption of the system allows the continuous operation for four weeks on a set of 1Ah batteries.

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