Vision Chip with High Accuracy Analog S^2I Cells

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***Abstract*— A mixed signal vision chip has been designed in a 0.18um 1P6M process. The chip incorporates a 256x256 array of processing elements, each element including 7 analog registers and 14 digital storage cells. By the programmable reconfiguration of these read/write storage elements, a compact and powerful processor array is enabled. Configuration options include setting up an array-wide analog diffusion network, and an asynchronous propagation network, allowing un-clocked inter-processor logic operations at 62x speed-up over synchronous equivalent operations. Analog registers degrade at ~1% of full-scale per second and show an offset error during a copy operation of 0.07% of register range.**

***Index Terms*—SIMD, Vision chip, parallel processing**

I. Introduction

VISION chips are generally composed of a number of processing elements (PEs) coupled closely to an imaging array. The PEs are normally programmed as SIMD processing units (all processors receiving the same instruction at the same time). For image pre-processing, the close proximity of processing nodes to a light transducer, with transducers embedded within the PE array, provides an arrangement that is highly conducive to fast and/or low power image analysis. However, the processor-per-pixel architecture does require compromises in the design of all components. The incorporation of memories (for frame and other data storage), an arithmetic logic unit, photodiode and communication systems requires that each sub-system fully justifies its silicon space, since it will automatically displace photodiode area and reduce PE count; the end requirement is the realization of the highest performance feasible within the footprint available. In order to achieve compact processing, data storage and light capture, analog processing in current-mode has been adopted by several designers. By this route, the analog memories serve the dual purpose of data storage and processing. This paper describes some in-usage examples of digital and analog operations of a recent vision chip.

II. Architecture

Each PE of our recent 256x256 vision chip (architecture of the system is shown in Figure 1) incorporates 6 general purpose registers (named A..F) and 1 special purpose register (named NEWS) - the latter having additional connectivity allowing inputs from neighbors and the squarer sub-system. Analog memories are implemented using S^2I cells. Other sub-systems include 13 DRAM digital memories, a comparator, a photodiode and a squarer [1]. Natively, the PE can add and invert analog data, and perform NOR, OR and NOT operations on digital data. The comparator enables a local flag (1-bit SRAM) to be set allowing subsequent operations to be dependent upon local values - this provides conditional functionality e.g.: IF $A_{i,j} > 0$ THEN $B_{i,j} \leftarrow C_{i,j}$ (A, B, C are 2-dimensional array registers with *i* and *j* taking values between 0 and 255).

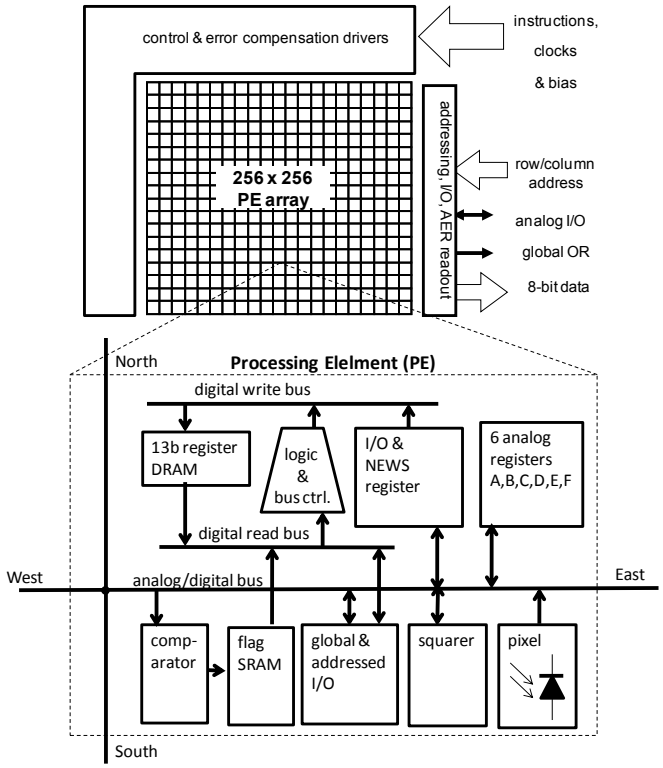

Figure 1. Architecture of the vision chip with 256x256 processor elements

An additional feature of the digital resources of the PE and the PE's connectivity is the ability to configure an asynchronous propagation network, whereby a wave of digital "1"s can be propagated from previously marked pixels within a defined propagation space. The wave will propagate within the space until impeded by cells loaded with "0"s [2]. Using analog resources and the same connectivity network as used for asynchronous propagation, local averaging (i.e. spatial diffusion) can also be enabled. The entire grid of analog buses

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is joined (by MOSFETs) with registers writing and reading from the grid. The finite resistance between PEs provides the local averaging. Diffusion is a single cycle operation.

III. Implementation and Results

The IC was fabricated using a 180nm 1P6M CMOS process, each PE occupying 32x32um, with die size of 10x10mm. The IC has a nominal operational instruction rate of 10MHz, with operations at 4.5MHz being optimal for analog operations. Most digital operations can be operated successfully at 16MHz. Photodiode fill factor is 6.2%.

1) Asynchronous propagation

Configuring the array as an asynchronous propagating network, allows operations such as hole filling and blob-extraction to be implemented. Propagation progresses from cell to cell in 3.2ns. This is demonstrated in Figure 2. An initial image of a maze is captured in 2(a) - the white lines define the barriers for the propagation wave; the wave is launched from a point in the bottom right hand corner of the image. The wave then propagates into all open spaces of the maze. This flood-filling operation can alternatively be operated by successive synchronous instructions; this requires a time 62x longer than the asynchronous equivalent.

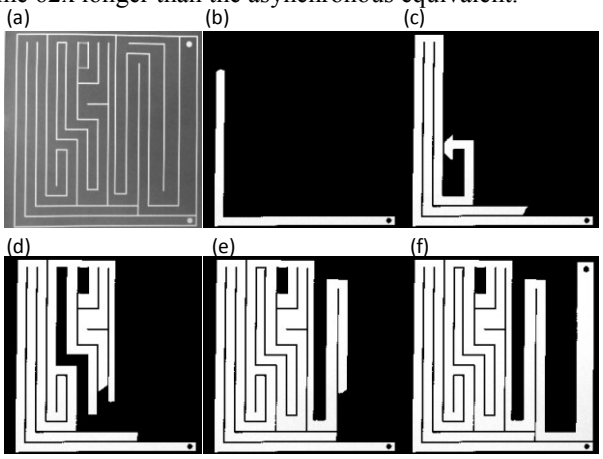

Figure 2. Operation of asynchronous propagation network through a maze. (a) Initial image, subsequently thresholded (b), Asynchronous propagation is started at bottom right corner. (c), (d), (e) and (f) show progress of propagation at successive intervals of 1.3us, with propagation complete in (f).

2) Analog register properties

The code stored in a register tends to shift (dependent on code) with time at a worst-case rate of 2.3%/s, but more typically at <1%/s. Degradation in stored data also occurs through the action of multiple operations; the copy operation adds a code dependent offset (0.07% of full-scale), a fixed pattern noise (0.05%) and a random noise (0.09%). The practical cumulative effect of these noise sources by the action of 25 copy operations (constituted from 50 inversion steps) is shown in figures 3 (b) and (e) from an initial image (figures 3(a) and (d)). The degradation over time of an analog register over 5s from the same source image is shown in Figures 3(c) and (f). As can be seen, the degree of data change for both extreme events is modest.

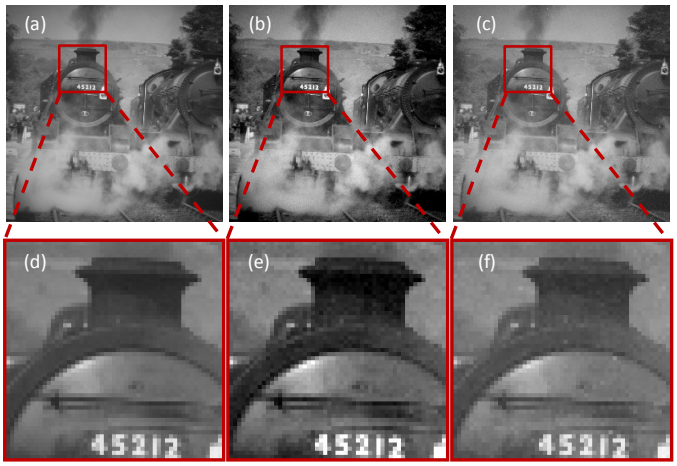

Figure 3. Effect on stored images due to register degradation and copy operations. (a) is the image as captured by the vision chip system, (b) is image after 25 copy operations, (c) is the data readout from the same register as initially sampled for image (a) but after a time delay of 5s. Images (d) (e) and (f) are expanded views of their respective 256x256 pixel images.

3) Diffusion

Two mechanisms are available for local averaging of register contents; the first uses a pair of MOSFETS configured as variable resistors, the other uses the NEWS register to short the analog buses of the array together. If a point source is considered, the FWHM of the two diffusion methods is ~1.75 and 4 PEs wide respectively. These methods are demonstrated in Figure 3.

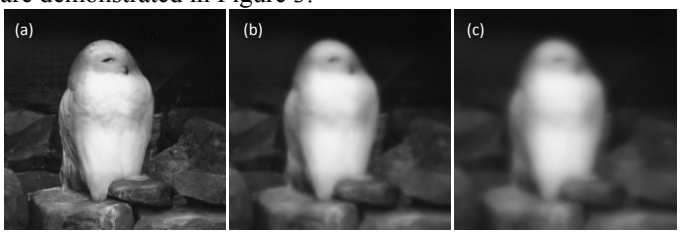

Figure 3. Diffusion operations. (a) Original captured image, (b) Diffused image using controllable diffusion network, (c) Diffusion via NEWS register connectivity

IV. Conclusions

A mixed signal vision chip with 256x256 processor elements has been designed. Each processor element contains reconfigurable connectivity allowing asynchronous digital operations and analog averaging to be conducted - permitting significant speedup over synchronous equivalent operations. Analog registers have long retention times (1% change per second) and show low signal dependence of error (0.07% of full scale).

V. Acknowledgments

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References

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