Anuj Vaishnav

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Education

2017 – 2020 PhD Computer Science, University of Manchester, UK.

Research Topic: *Resource Management and FPGA Virtualization for Cloud*.
Supervised by: *Dr. Dirk Koch* and *Dr. James Garside*

Research focus: Transparent elastic resource sharing among hardware accelerators for maximising resource utilisation, performance and energy efficiency. It would allow users to deploy their custom hardware accelerators described in OpenCL/C to the cloud with ease and high performance.

2014 – 2017 BEng (Hons) Computer System Engineering, University of Manchester, UK.

First class degree with *85%* and specialisation in *System-on-Chip* and *Computer Architecture*.

- Final year project: Designing and implementing a security library of custom hardware instructions for high-performance acceleration using vectorised FPGA interlays.
- Final year modules: Chip Multiprocessors, Implementing System-on-Chip Designs, Agile Software Engineering, Compilers, Cryptography and Networks Security, and Documents on the Web.

Awards*:*

- ***President's Doctoral Scholar Award, University of Manchester – 2017-21***
  Given to the *top 3%* of research students across the university who demonstrate academic excellence and leadership potential.
- ***Edwards Prize, University of Manchester – 2016-17***
  For the *highest distinction* in examinations, laboratories and projects relating to Computer Engineering courses throughout the degree.
- ***IBM Team Challenge Award, University of Manchester – 2015-16***
  For the consistent sterling performance of the *team* on all Software Engineering coursework.
- ***Golden Anniversary Prizes, University of Manchester – 2014-15***
  For Excellence in first-year studies. Given to *top 5* students of the year.
- ***Kate Kneebone Acorn Bursary, University of Manchester – 2015-16***
  For a student with academic merit who has shown commitment, determination, enthusiasm, personal application and promise.

Research Experience

2015 July-Aug Summer Research Assistant, APT Group, University of Manchester, UK.

Skills gained: Expertise in Transport Triggered Arch. and Dataflow models, Technical report writing.

- Designing computer architecture based on Dataflow and Transport Triggered Arch.
- Writing technical reports based on analysis of design and research papers.
- Building functional simulator of the resulting computer architecture in JAVA for experimentation.

Experience

2016 July-Sept Hardware Intern – Design & Verification, ARM

Verification IP team intern for AMBA protocols (CHI, ACE, AXI) and its future variants.

- Improving current systems for better functional coverage checking.
- Integrating new AMBA features in verification test-benches.
- Creating new regression work-flow for lint tool and its continuous integration.
- Reporting and resolving bugs in work-flow and verification test-benches.

Selected Publications

- [Accepted/In press] **A. Vaishnav**, K.D. Pham and D. Koch, "*Live Migration for OpenCL FPGA Accelerators*", FPT, Naha, 2018. **(*Best Paper Nominee)**
- K.D. Pham, **A. Vaishnav**, M. Vesper, D. Koch, "*ZUCL: A ZYNQ UltraScale+ Framework for OpenCL HLS Applications*", 5th FSP, Dublin, 2018.
- **A. Vaishnav**, K.D. Pham and D. Koch, "*A Survey on FPGA Virtualization*", 28th FPL Dublin, 2018.
- **A. Vaishnav**, K.D. Pham, D. Koch and J. Garside, "*Resource Elastic Virtualization for FPGAs using OpenCL*", 28th FPL, Dublin, 2018.
- **A. Vaishnav,** J. R. G. Ordaz and D. Koch, "*A Security Library for FPGA Interlays*", 27th FPL, Ghent, 2017.

Full list available on Google Scholar: https://scholar.google.co.uk/citations?user=GIMybIcAAAAJ

Positions of responsibility

2014 – 2016 Board member of School of Computer Science Committee, University of Manchester, UK

Skills gained: Communicating between the school management team and students, Adapting different working structures, Formulating new policies.

- Evaluating concerns of students and staff members.
- Formulating, analysing and implementing new policies.
- Discussing working pattern of school and improving course units.

Skills

Hardware:	Verilog • Vivado HLS • Vivado • ISA simulation • Verification test-bench • ARM assembly • Functional Coverage • AMBA protocols • FPGA modelling
Object-oriented lang.:	Java • Python • Ruby • Matlab
Procedural languages:	C
Website development:	HTML + CSS • PHP • SQL • XSL
OS & other software:	OpenCL • Bash • Tcsh • Android • GNU/Linux • Windows • Gitlab • SVN • Atlassian JIRA • Atlassian Bamboo • JUnit Testing • LATEX

Projects and Interests

- Processor/System simulation at High-level (JAVA) and RTL (Verilog: MIPS I, ARM 32b Subset, MU0).
- Second-year team project – Improving open source Stendhal game base: bug fixes, new features and refactoring existing code base with testing.
- Organising postgraduate summer research symposium (PSRS) for entire University of Manchester research community.