Unidirectional electron flow in a nanometer-scale semiconductor channel:
A self-switching device

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By tailoring the boundary of a narrow semiconductor channel to break its symmetry, we have realized a type of nanometer-scale nonlinear device, which we refer to as self-switching device (SSD). An applied voltage \( V \) not only changes the potential profile along the channel direction, but also either widens or narrows the effective channel depending on the sign of \( V \). This results in a diode-like characteristic but without the use of any doping junction or barrier structure. The turn-on voltage can also be widely tuned from virtually zero to more than 10 V, by simply adjusting the channel width. The planar and two-terminal structure of the SSD also allows SSD-based circuits to be realized by only one step of lithography. © 2003 American Institute of Physics.

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Advancing semiconductor technology has allowed for a single chip to contain a billion devices and operate at GHz frequencies. With the device feature sizes coming down rapidly to about 100 nm, it has been predicted that the miniaturization of conventional semiconductor devices will soon reach its limit, and the future generations of electronic devices will have to be built with nanoscience and technology based on different device concepts. At the nanometer scale, transistor structures, such as the single-electron transistor (SET),\(^1\)\(^-\)\(^3\) and lateral gate transistor,\(^4\) have been invented. A SET possesses properties such as low power consumption and ultrahigh sensitivity, while the lateral transistor promises very simple design and one-step fabrication. Aiming at practical applications, great efforts have been made to fabricate SETs that can operate at room temperature.\(^5\)\(^-\)\(^7\)

Apart from these transistor concepts, possible nanometer-scale counterparts of conventional diodes were also investigated. Two particular examples are the ballistic rectifier\(^8\) and three-terminal ballistic junction.\(^9\),\(^10\) The room-temperature and high-frequency (up to 50 GHz) operations of both devices have been demonstrated, showing promising possibilities of practical applications.\(^11\)\(^-\)\(^13\) Nevertheless, the working principles of both devices rely on ballistic electron transport, which is why so far room-temperature devices were fabricated only on high-mobility III–V semiconductors but not silicon.

Here, we propose and demonstrate a different type of nanometer-scale, nonlinear structure, which we refer to as a self-switching device (SSD). Not only has it been demonstrated using two types of III–V semiconductors, we also expect it to be reliably fabricated using silicon by the current complementary metal–oxide–semiconductor (CMOS) technologies. Also, different from the ballistic rectifier and three-terminal ballistic junction mentioned above, a SSD has only two terminals. The current–voltage characteristic is similar to that of a conventional diode, but the turn-on voltage can be widely tuned by simply changing the designed device channel width. Unlike in a diode, neither a doping junction nor tunneling barrier is needed in a SSD for its nonlinear property. The different working principle allows SSDs and SSD-based simple circuits to be made by only one step of lithography.

The SSDs were fabricated using two material systems: a modulation-doped In\(_{0.75}\)Ga\(_{0.25}\)As/InP quantum-well wafer grown by metal organic vapor phase epitaxy and two modulation-doped In\(_{0.53}\)Ga\(_{0.47}\)As/In\(_{0.53}\)Al\(_{0.47}\)As heterostructures, lattice matched to InP substrates, grown by molecular beam epitaxy. The InGaAs/InP structure consists of a two-dimensional electron gas (2DEG) in the quantum well, about 40 nm below the surface. The sheet carrier density and mobility at temperature \( T = 4.2 \) K are \( 4.5 \times 10^{15} \) m\(^{-2}\) and \( 45 \) m\(^2\)/V/s, respectively, and at room temperature \( 4.7 \times 10^{13} \) m\(^2\)/V/s, respectively. The 2DEGs in the two InGaAs/InAlAs wafers are about 50 nm below the surface, and at room temperature the carrier density and mobility in wafer A are \( 1.0 \times 10^{16} \) m\(^{-2}\) and \( 1.0 \) m\(^2\)/V/s, and in wafer B are \( 1.5 \times 10^{16} \) m\(^{-2}\) and \( 1.1 \) m\(^2\)/V/s.

The key fabrication of the SSDs was to create insulating grooves by standard electron-beam lithography and wet chemical etching. Figure 1(a) is a typical scanning electron micrograph, in which the dark areas (two lines) were etched through the 2DEG layer and became insulating. This results in a narrow channel (width \( W \approx 60 \) nm) between the
trenches. The continuation of the trenches to the device boundary broke the symmetry and ensured that the current \( I \) could flow only via the channel. As shown in Fig. 1(b), the effective channel width was actually smaller because of the depletion region at the etched boundaries, which was caused by the charges at surface states. If a positive voltage \( V \) is applied between the right and left contacts (referred to as a positive bias in this letter), the effective channel width will increase because of the electrostatic field effect from both sides of the narrow channel, which in turn effectively reduces the depletion length as shown in Fig. 1(c). If \( V<0 \), however, the field effect from the bias-induced negative charges on both sides of the channel will reduce the effective channel width and possibly even completely pinch off the channel, as illustrated in Fig. 1(d). The above mechanism leads to a preferred direction of electron flow and gives rise to the diode-like functionality.

Figure 2 plots the \( I-V \) characteristics of two InGaAs/InP-based SSDs with the same channel length \( L=1.2 \mu m \) but different channel widths \( W \), measured at 4.2 K. The first device exhibited a virtually zero turn-on voltage \( (V_t<10 \text{ mV}) \). This suggests that when \( V=0 \), the channel was close to a complete pinch-off, i.e., \( W=80 \text{ nm} \) was just about twice the depletion length. In the second device, the channel was fully pinched off under the equilibrium condition, and a positive voltage of 0.9 V was needed to drive a current through the channel. In fact, many more devices with different geometric parameters have been fabricated, and virtually all devices exhibited such diode-like characteristics. Although the fabrication was close to the limit of our electron-beam lithography, the reproducibility was good since \( V_t \) normally varied within 30\% for a given \( W \). As expected, the narrower the channel width, the higher the turn-on voltage. Hence, specific channel widths can be designed to meet different requirements.

Apart from the apparent differences in device structures, the SSD is also based on a completely different working principle from a conventional diode since neither doping junction nor barrier structure was used along the current direction in the SSD. More importantly, only one step of lithography was needed. This can significantly reduce both the cost and difficulty of modern lithography processes due to the multiple steps of mask alignment of \( \sim 100 \text{ nm} \) features, which require an increasingly challenging alignment precision below \( \sim 20 \text{ nm} \).

SSDs were also fabricated on the InGaAs/InAlAs wafers and showed similar properties to InGaAs/InP-based SSDs. The results confirmed that \( V_t \) can be tuned simply by changing \( W \). Figure 3(a) plots the room-temperature \( I-V \) characteristics of two SSDs. While we did not observe any leakage current above 1 nA up to \( V_t=-3 \text{ V} \) from the first SSD, of which \( W=60 \text{ nm} \) and \( V_t=1.0 \text{ V} \), the other device exhibited a nearly ideal turn-on voltage \( V_t=0 \) but also an undesirable leakage current. We believe that the leakage was largely due to the limitations of our fabrication. The wet etch led to very wide trenches (\( \sim 300 \text{ nm} \) in Fig. 1), which significantly limit the bias-induced transverse electric field, and hence, also the extent of the widening and narrowing of the channel. Improved lithography with better pattern definition and dry etch will not only achieve much smaller devices but also remarkably reduce the leakage current.

The temperature dependence of the second device is shown in Fig. 3(b). Although some change in the \( I-V \) characteristics was observed as the temperature increased from 100 K to room temperature, it was much less than the exponential temperature dependence of a \( p-n \) diode. In fact, the characteristics hardly changed between 20 and 100 K, bearing a resemblance to a tunneling diode. A remarkable difference is, however, that the current actually reduced with increasing the temperature, meaning that SSDs could also be used, e.g., for compensation of temperature changes in practical circuits.

In Figs. 2 and 3, the channel resistance is generally above 100 k\( \Omega \) even under the forward-bias condition. So far in the literature, there are very limited studies on narrow...
channels in such a nearly pinched-off regime, particularly under large-bias conditions. Furthermore, once a finite voltage is applied to a SSD, the additional transverse electric field varies along the channel direction. A full model needs to include a self-consistent calculation of the three-dimensional potential profile and most likely also the tunneling and hot electron effects, which is beyond the scope of this letter.

The device operation does not rely on the ballistic electron transport, since at room temperature the mean-free path of the two-dimensional electrons is an order of magnitude shorter than $L$. The SSD, hence, fundamentally differs from the ballistic rectifier and three-terminal ballistic junction.\textsuperscript{5–10} The weak temperature dependence shown in Fig. 3(b) confirms that the device operation does not require a high electron mobility, as was anticipated from the working principle. These facts convinced us that SSDs can also be produced using silicon materials by the advanced CMOS technologies, which would greatly enhance the possibilities to practically use SSDs.

One of the most significant properties of the SSD is the remarkably simple lithography, i.e., requiring only to create insulating lines on a piece of semiconductor, like the fabrication of a lateral gate transistor.\textsuperscript{4} In fact, by extending one of the trenches of a SSD, an additional gate can be formed, as shown in Fig. 4(a). This results in a different device with the \textit{combined functionalities} of the SSD (as a diode) and lateral gate transistor. Such a self-switching transistor (SST) opens more possibilities for real applications. For example, if used as a transistor, a SST may provide two different characteristics, depending on the sign of the source-drain voltage, $V_{SD}$. If used as a diode, the threshold of the SST can be tuned continuously by the gate voltage.

Being a planar, two-terminal [or three-terminal as in Fig. 4(a)] device, SSD is a flexible element in constructing circuits without or with reduced interconnect (bridging) problems. This can be illustrated, for example, by a SSD-based bridge rectifier and an additional design for higher current operations in Figs. 4(b) and 4(c). Both circuits can be fabricated in only one step, too. Another example is demonstrated in Fig. 5, where a simple logic OR gate was constructed by two SSDs. The experimental results in Fig. 5(b) show that by varying the two input voltages separately, the simple circuit, created by a few trenches, could produce the OR functionality with an output/input ratio of about 80\% at room temperature. This, again, demonstrates that SSDs may provide remarkable simplicity and flexibility in circuit design and fabrication.

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