Room-temperature operations of memory devices based on self-assembled InAs quantum dot structures

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Memory devices have been fabricated in high-electron-mobility transistors with embedded InAs quantum dots (QDs). We show that memory operations can be fully controlled by gate biases at room temperature, without the need for light excitations to erase memory states. Real-time measurements indicate a charge retention time of a few minutes. Neither such retention time nor the self-consistent simulations can justify the picture that the memory effect is due to charging/discharging of intrinsic QD states. Experiments at a series of gate biases point to the presence of deep levels coexisting in the QD layer(s), which are responsible for the memory effect. © 2004 American Institute of Physics. [DOI: 10.1063/1.1831558]

Self-assembled semiconductor quantum dots (QDs), created by epitaxial growth in Stranski–Krastanow mode, have been intensively studied because of their importance to device applications and in fundamental physics. Most investigations have focused on optoelectronic devices such as lasers, light emitting diodes, and photodetectors. Among the advantageous device properties that are based on the discrete energy states are low threshold current for light emissions, efficient coupling to normal incident lights, and additional tunability of emission/detection wavelength. Recently, the possibilities to design electronic memory devices using QD structures have attracted increasingly notable attention. Perhaps the simplest design is to embed quantum dots in the close vicinity to the two-dimensional electron gas (2DEG) in a high electron-mobility-transistor (HEMT) structure, and the QDs are charged/discharged by changing the gate bias. It was expected that if electrons were transferred from the 2DEG to charge the QDs, not only was the 2DEG density reduced but also the negatively charged QDs could lower the conductance of the 2DEG by Coulomb scatterings. As a result, the charging or discharging of the QDs and therefore the change in the memory states could be monitored by the source–drain conductance. A potential advantage is that the electric current and therefore power consumption required for memory operations in a QD-based memory device could be substantially lower than in a conventional memory cell, because of the single-electron charging effect. Whereas a conventional memory cell, the charging or discharging of the QDs and therefore the conductance of the 2DEG by Coulomb scatterings. As a result, the charging or discharging of the QDs and therefore the change in the memory states could be monitored by the source–drain conductance. A potential advantage is that the electric current and therefore power consumption required for memory operations in a QD-based memory device could be substantially lower than in a conventional memory cell, because of the single-electron charging effect. Whereas a cluster of defects in a conventional dynamic memory or a flash memory could cause a rapid discharge of the whole capacitor plate or charge-storage floating gate, such problems are absent in QD-based memory devices. An accidental discharge in one dot would not affect the charges in other dots since they are spatially separated from each other. Moreover, these devices do not require hot electrons to charge the QDs, allowing low operation voltages to be used.

From the application point of view, however, both room-temperature and fully electrically controlled memory operations are essential. Furthermore, hardly any time-domain experiment has been carried out to characterize the memory holding time, despite it being one of the most important parameters of memory devices. From the physics point of view, the energy states that were involved in the charge and discharge processes have not been particularly studied.

In this work, we fabricated memory devices using three pseudomorphic InGaAs–AlAs or InGaAs–AlGaAs HEMT structures, with either a single layer or five layers of InAs QDs. Both room-temperature and fully electrically controlled memory operations were demonstrated, with charge retention times up to a few minutes. Self-consistent simulations on conduction band profiles and experiments on gate voltage dependence have also been carried out, in order to identify the energy states involved in the memory operations.

Figure 1 shows the schematics of two of the wafers in our experiments, grown by solid-source molecular beam epitaxy. Both wafers, Nos. 1681 and 1693, consist of an inverted HEMT structure with a strained In_{0.15}Ga_{0.85}As quantum well. Whereas one layer of two-monolayer InAs dots were embedded in No. 1693, five layers, spaced by 10 nm Al_{0.3}Ga_{0.7}As layers, were grown in No. 1681. The third wafer, No. 1701, is similar to No. 1693 but it has a thicker AlGaAs barrier between the gate and the QD layer, and a lower 2DEG density. Room-temperature Hall measurements yielded that the 2DEG density and the mobility were 1.6 × 10^{12} cm^{-2}, 4800 cm²/V·s in No. 1693, and 1.2 × 10^{12} cm^{-2}, 3200 cm²/V·s in No. 1681, respectively. The actual presence of quantum dots was investigated by room-temperature photoluminescence measurements, and the QD density was determined by imaging an unencapped sample with an atomic-force microscope (AFM), as shown in the insets in Fig. 2. Standard HEMT lithography, involving wet etching, Au/Ge/Ni ohmic contacts annealed at 450 °C, and Au gate, was performed. The gate length was 5 μm and the widths ranged from 10 to 100 μm. The gap between the gate and the source–drain ohmic contacts was 5 μm. A typical transistor characteristic of the devices at room temperature is shown in Fig. 2.
The memory operations of the devices were characterized in both hysteresis and real-time measurements. The drain current $I_{DS}$ versus gate voltage $V_{GS}$ in Fig. 3(a) was measured at a fixed drain voltage $V_{DS}=0.5$ V. The hysteresis is similar to the results reported by other groups.\(^7,8,10\) In a control sample that had a similar structure to wafer 1693 but without embedded QDs, no appreciable hysteresis was detected, indicating that the QD layer was responsible for the memory effect. The common explanation of the hysteresis was based on the charging and discharging of the intrinsic QD energy states. In such a picture, when $V_{GS}$ starts with a positive value, the potential at the QD layer is lowered and the dots are charged by electrons from the 2DEG. The reduced 2DEG density results in a lower conductance when $V_{GS}$ is swept downwards, as reflected by the lower-current trace in Fig. 3(a). Depending on the dot density and the distance between the QD layer and 2DEG, the charged dots could also scatter the 2DEG by Coulomb interactions, leading to a further reduced 2DEG conductance. When $V_{GS}$ is swept upwards, the QDs have been discharged at negative gate voltages, leading to the higher-current curve in Fig. 3(a). Whereas such a picture is rather appealing, it was not supported by our potential profile analysis and could not explain the experimental results in Fig. 4, which will be discussed in the following.

The memory operations of the devices were demonstrated in real-time measurements of $I_{DS}$ during which $V_{DS}$ was fixed at 100 mV. The results that consist of three charging/discharging operations are shown in Fig. 3(b). First, a negative $V_{GS}$ pulse of $-4$ V was applied for 1.0 s (writing a higher-conductance memory state) to discharge the electronic states that were above the Fermi energy of the 2DEG, $E_F$, under this bias condition. The $I_{DS}$ decay was then recorded when it was decreasing toward its initial value (reading process). To write a lower-conductance memory state to the device, a positive pulse at $+2$ V was applied to the gate to recharge the electronic states that are now below $E_F$, followed by the recording of the drain current. Since the charged states were below $E_F$ and hence remained stable, $I_{DS}$ did not change with time as shown by the flat $I_{SD}$ curve. In the above-mentioned experiment, the default gate voltage was $-1$ V. During $V_{GS}$ pulses $I_{DS}$ was not recorded. The use

**FIG. 1.** (Color online) The growth structures of two wafers, Nos. 1681 and 1693, in our experiments and corresponding conduction-band profiles at zero gate bias.

**FIG. 2.** (Color online) Typical characteristics of a HEMT fabricated from wafer 1681. The result of room-temperature PL and an AFM image are shown in the insets.

**FIG. 3.** (Color online) Hysteresis and real-time operations of a memory device at room temperature.

**FIG. 4.** (Color online) Gate-bias dependence of the decay of $I_{DS}$ at room temperature. $V_{DS}$ is fixed at 100 mV during the measurements.
of 1.0-s-long $V_{GS}$ pulses was for the ease of measurements and clarity of the representation. The pulses can be orders of magnitude shorter. Separate experiments showed clear hysteresis when the gate bias was swept at frequencies up to at least 50 kHz. Compared with a floating gate memory device in which the whole floating gate has to be charged or discharged, our device only requires charging the deep levels, the cross section of which is orders of magnitude smaller. Furthermore, each deep level only accommodates a few electrons, allowing a very quick charging process and therefore memory erasing and writing time. Depending on the QD density our memory device can be downsized until it contains only a few QDs.

A charge retention time on the order of minutes can be determined in Fig. 3(b). This is much lower than that of a flash memory, but orders of magnitude longer than the memory holding time ($\sim$1 ms) of a typical dynamic RAM. Obviously, the flexibility in layer thickness and material composition of such or similar compound semiconductor structures provides plenty of room for significant improvements.

Another important aspect for performance improvements as well as fundamental device physics is to identify and understand the energy states that are responsible for storing (releasing) electrons in the charging (discharging) process. For this purpose, we carried out self-consistent simulations, using a Green’s functions simulator called WinGreen. Figure 1 plots the conduction band profiles at zero gate bias. The approximate positions of the QD energy levels (s and p states), marked in the diagrams, were taken from the recent deep-level transient spectroscopy (DLTS) experiments. The conduction band profiles clearly show that the actual intrinsic QD energy states lie well above $E_F$ at zero gate bias, which is more so during the memory operations where $V_{GS}$ $<$ 0 V. Furthermore, even if the QD states were charged, the thermal emission time, estimated using the results of DLTS experiments, would be on the order of nanoseconds at 300 K, more than ten orders of magnitude shorter than what we observed. We therefore rule out the possibility that the intrinsic QD states are responsible for the memory effect.

To identify the energy states that were actually involved in the memory operations, we performed gate-bias-dependence experiments. Figure 4 shows $I_{DS}$ decays of a No. 1693 device recorded immediately after different gate voltage pulses. A relatively fast decay can be identified in the first tens of seconds, but a much slower process dominates as long as the gate pulses are more negative than a threshold of about $-1.0$ V. Self-consistent simulations at $V_{GS}=-1.0$ V indicated that the Fermi level of the 2DEG is 0.72 eV below the s states of the QDs, that is 0.87 eV below the GaAs conduction band edge. We conclude that this is the level position of the energy states that are responsible for the memory effect. Similar results were obtained in samples fabricated from wafers 1681 and 1701, and the energy positions of the states that were aligned with $E_F$ at the corresponding thresholds were consistent after taking into account the conduction band difference between GaAs and AlGaAs. The fact that no memory effect was observed in a control sample that had no QDs embed strongly suggests that these states coexist in the QD layer, which might be induced by, e.g., strain. To further confirm this, we performed separate DLTS experiments on structures under the same growth conditions (results to be reported elsewhere). The excitation energy of the QD s states was determined to be about 150 meV, and deep levels with a fairly broad energy distribution and excitation energy around 0.5 eV were identified to indeed coexist in the same layer as QDs.

To conclude, we have demonstrated room-temperature, fully electrically controlled memory devices based on QD structures. We pointed out the existence of deep-level states. Further studies on these states not only are important for material growth and physics, but also could open other possibilities for novel device applications.

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