Analogue CMOS Circuit Implementation of a Dopamine Modulated Synapse

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Abstract— This paper describes a synapse circuit that approximately implements the dynamics of the dopamine (DA) modulated synapse proposed by Izhikevich (2007). The dynamics of the model, based on 'eligibility traces' generated according to a spike-timing-dependent plasticity (STDP) rule, ensure that causal pre-/post- synaptic spiking activity in the time preceding the reward, signaled by DA, leads to strengthening of the synaptic connections. The circuits are designed and fabricated in a 0.35 µm CMOS technology and the simulation results are presented. This circuit block is a good candidate for the development of neuromorphic VLSI architectures that implement brain-inspired computation using biologically plausible reinforcement learning strategies.

I. INTRODUCTION

Dopamine (DA) is a neuromodulator in the nervous system that regulates diverse populations of neurons. Dopaminergic neurons are closely associated with reward-seeking behaviours; the brain areas where these neurons are present are known to carry functions such as working memory, learning, and attention [1]. Even though these neurons are found in few brain regions only, their projections are generally highly diffuse and reach large portions of the brain [1]. The burst stimulation of the dopaminergic neuron releases DA globally to many DA modulated synapses. This increases the extracellular DA concentration at the synapses enhancing their long-term potentiation (LTP) and/or depression (LTD) [2, 3]. This effect of DA plays a major role, in particular, in reinforcement learning.

In this paper, we propose a synapse circuit broadly based on the DA modulated synapse model proposed by Izhikevich [4]. The LTP and LTD components of the spike-timing-dependent plasticity (STDP) are modulated by DA present during the critical window of a few seconds after the post synaptic spike. According to the model, the strength of the synapse, *s,* evolves as per the following three equations [4]:

$$\dot{c} = -c/\tau_c + STDP(t_{post} - t_{pre})\delta(t - t_{pre/post}) \quad (1)$$

$$\dot{s} = cd \quad (2)$$

$$\dot{d} = -d/\tau_d + DA(t) \quad (3)$$

In the above equations c is the synaptic eligibility trace (ET); $\delta(t)$ is the Dirac-delta function that provides a step-increase or decrease of c depending on pre- and post- synaptic neuron firing times, t_{pre} and t_{post}; the function $STDP()$ describes the spike-timing-dependent change of the ET (typically, the change has a positive value when post-synaptic spike follows a pre-synaptic spike within a small time interval, negative value when post-synaptic spike precedes the pre-synaptic one, and decays to zero for larger pre- and post- synaptic spike time differences); d represents the extracellular concentration of DA, $DA(t)$ is the amount of the DA released due to the activities of the dopaminergic neurons. Time constants, τ_c = 1 s and τ_d = 0.2 s. Dynamics that are described by these equations are further explained in [4].

The model addresses a solution to the distal reward/credit assignment problem using DA modulation of STDP; only nearly coincident spiking patterns occurring in the time period before the reward are reinforced by the reward, whereas uncorrelated spikes occurring before the reward, and correlations when no reward is present, are ignored by the network. The spike coincidences produce relevant changes in the slowly decaying eligibility traces, and the eligibility traces control changes in the synaptic strength, making the greatest influence when the reward signal (DA activity) is strong.

II. PROPOSED CIRCUIT

To build a VLSI neural network, a compact implementation of circuit blocks is a core requirement. When developing the spiking/bursting cortical neuron circuit [5] we have adopted the strategy of approximating established neural models in CMOS using different (and usually more complicated) model equations, but very simple circuit implementations. We are continuing this strategy in the present work, and propose a CMOS circuit that provides a qualitative behaviour similar to the model described above, more complex in its analytical formulation, but compact in terms of physical circuit implementation. The circuit has been implemented in a standard CMOS 0.35 µm technology. While it is usual for neuromorphic circuits [6] to operate in "biological real time" (i.e. emulate the behaviour of neural circuits on a time scale identical with the actual neuronal activity), we follow the strategy of using "accelerated time"

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emulation, thus providing higher computational throughput of the neuro-mimetic computing device [7]. The dynamics of the proposed circuit are approximately three orders of magnitude faster than biology – the same time scale as of our previous circuits [5]. The DA modulated synapse circuit comprises of three sub-circuits: the eligibility-trace (ET) circuit, the synaptic strength circuit and the output circuit; the circuit schematics are shown in Fig .1 and Fig. 2. The DA modulated synapses receive DA signal from the common DA generator circuit shown in Fig. 3.

A. Elegibility-Trace Circuit

The eligibility-trace circuit (Fig. 1) generates potentiating and depressing parts of the ET separately using two sub-circuits: long-term eligibility potentiation (LTEP) and depression (LTED) circuits. The design of these circuits is similar to the STDP synapse circuits proposed by Indiveri [8]. The capacitors MCwp and MCwd store the potentiation (*ETp*) and depression (*ETd*) information of the ET respectively. Firings of the pre- and post- synaptic neurons induce changes to the *ETp* and *ETd*, implementing the STDP rule. If the DA is present, these synaptic changes will result in modification of the synaptic strength, *S,* (produced in the synaptic strength circuit) during the critical window of a few milliseconds (equivalent to a few seconds in biological time) before the *ETp* and *ETd* decay to zero.

The signal *pre_bar* is the inverted pre-synaptic firing signal where as the signal *post* is the post-synaptic firing signal. Once the pre-synaptic neuron fires, the capacitor MCltp is charged to *Vdd* by switching-on the transistor M3p. The capacitor is then continuously discharged with a "leakage" current, through transistors M1p and M2p. The amount of charge removed from MCltp is approximately proportional to the time after the last pre-synaptic neuron firing. The maximum time duration for the capacitor to discharge to a voltage low enough to force the gate voltage of the transistor M4p to reach its cut-off region of operation is equivalent to the '*LTP time window'*. This is controlled by the voltage *Vlkp*. If a post-synaptic spike follows the pre-synaptic firing within the LTP time window, the LTEP circuit increases the charge in the capacitor MCwp by switching-on the current path through the transistors M6p, M5p and M4p. The voltage *Vp* limits the maximum current through these transistors. The eligibility-trace *ETp* decays to *Vdd* through M7p-M8p. The speed of decay is controlled by the voltage *VlkWp*.

The LTED circuit has a complementary topology to the LTEP circuit. Both outputs signals of the ET circuit, *ETP* and *ETD,* are provided to the synaptic strength circuit to produce the synaptic strength change. When the pre-synaptic neuron fires, the synaptic strength, *S,* regulates the amount of post-synaptic current *(PSI)* injected to the post-synaptic membrane.

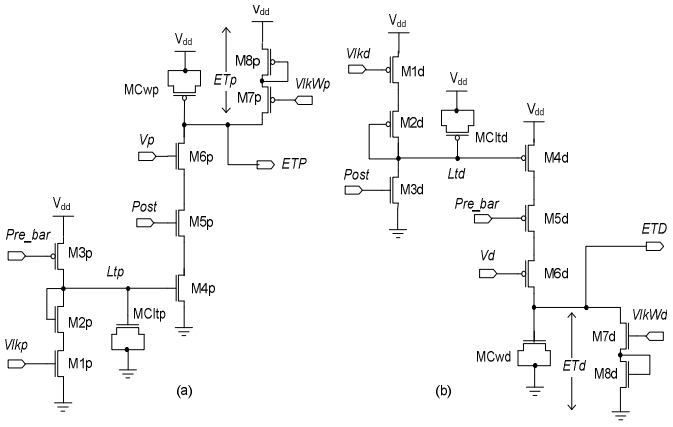

Fig. 1. Eligibility trace circuit: (a). LTEP circuit; (b). LTED circuit.

B. Synaptic Strength Circuit

The synaptic strength circuit (Fig. 2) receives the eligibility-trace signals the *ETP* and *ETD* from the ET circuit, and the DA pulse signal, *DAP,* and its inverted signal, *DAP_bar,* from the DA generator circuit. The circuit parts for the synaptic strength potentiation and depression, shown in Fig. 2 (a), are complementary. When considering the potentiation part of the circuit, during the time *DAP_bar* is low, the potential divider (transistors M1p, M3p-M4p) creates a potential at *Sp* proportional to the *ETp* voltage. The pulse width of the *DAP_bar* signal is proportional to the amount of DA. Hence, the amplitude and the width of the signal *Sp* of the synaptic strength circuit carries the *ETp* and DA level information respectively. The M6p transistor can operate either in the sub-threshold or in the linear range depending on the externally controlled voltage, *Smp*. If the transistor M6p (M6d) is biased to operate in the sub-threshold region, the charge through the M6p and M7p (M6d and M7d) is proportional to the product of the DA level and the exponential of the eligibility traces, *ETp* (*ETd*). Hence in this case, the net charge increase at the capacitor, MCs is proportional to the product of the DA-level and $e^{(ETp-ETd)}$.

If the transistor is biased to operate in the linear region, then the charge through the M6p and M7p transistors (charging the capacitor Mcs) is proportional to the product of the DA level and the *ETd* voltage. The depression circuit M1d-M7d works in the same way to discharge the capacitor MCs. Hence the net charge increase at the capacitor, MCs which stores the synaptic strength, is proportional to the product of the DA-level and the *ETp-ETd* voltage difference.

Once the pre-synaptic neuron fires, the synaptic output circuit creates a post-synaptic current (*PSI*) as a function of the synaptic strength, *S.* The externally controlled *PSI_ctl* voltage limits the PSI current flow to the membrane of the post-synaptic neuron.

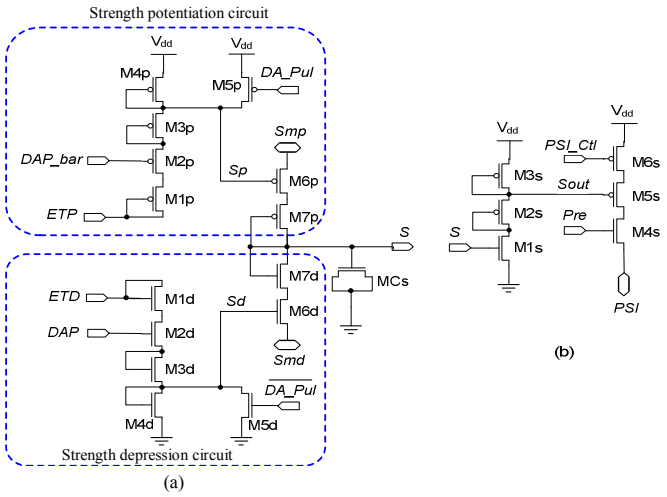

Fig. 2. (a) Synaptic strength circuit and (b) Synapse PSI output circuit.

C. DA Generator Circuit

The DA generator circuit (Fig. 3) provides the DA pulse signal to the DA modulated synapses in order to update the strengths of the synapses. The level of extracellular DA (which is represented by the voltage *Da* referenced to *Vdd*) is increased by a burst of spikes provided at the gate of the M1 transistor. This burst of spikes is assumed to be provided from a bursting neuron output as a consequence of the reward prediction clue or reward-triggering action. After the burst, the DA level decays to *Vdd* through the transistor M3. The time constant of the decay can be controlled using the voltage *VlkDA*. The DA level is buffered to the node *Dab* using the source follower (M4 and M5) and is provided to the transmission gate TR1. The transmission gate is switched periodically using an externally controlled clock signal *DA_Clk*. When the TR1 is 'ON' the parasitic capacitance at the node *Dat* is charged to the voltage at node *Dab*, and the transistors M9 and the M10 are switched 'OFF' and 'ON' respectively. This creates the rising edge of the DA pulse (*DAP*). Then the parasitic capacitor is discharged through the transistors M6 and M7. The speed, at which this capacitor is discharged, is controlled by the voltage *Vlk*. If the *Vlk* is kept at a fixed voltage, the time taken to discharge the capacitor such that the transistors M9 and the M10 are switched 'ON' and 'OFF' respectively, is approximately proportional to the level of DA (*Da*). Therefore, the pulse width of the *DAP* signal is proportional to the DA level. The buffer at the output is used to provide faster rise and fall times for the *DAP* signal.

III. Simulation Results

The above circuits are simulated in a standard 0.35um CMOS technology and results are presented in Fig. 4 and Fig. 5. Fig. 5 shows the STDP curves generated from the eligibility trace circuit shown in Fig. 1. The STDP curves can be adjusted using control voltages *Vp*, *Vd*, *Vlkp* and *Vlkd*. Fig. 5 (a) and (c) shows the effect on the magnitude of changes to the voltage *ETp* (*ΔETp*) and the *ETd* (*ΔETd*) when *Vp* and the *Vd* is varied respectively. Fig. 5 (b) and (d) shows how LTP and LTD time windows can be varied by varying the voltages *Vlkp* and *Vlkd* respectively. In a practical circuit, the device mismatch will also affect these characteristics. It should be noted that *ΔETp* and *ΔETd* also depend on the value of *ETp* and *ETd* respectively; the plots in Fig. 5 are generated when the *ETp* and *ETd* are at their mid values.

Characteristics of the synaptic strength circuit (Fig. 2) are shown in Fig. 4. The amount of change in strength (*Delta S*) is plotted as a function of *ETp*/*ETd* value and *DAP* pulse width for a single update of strength. The frequency of update can be set by changing the DA clock frequency (using the *DA_Clk*). Further, the amount of increase or decrease in *S* per single update, for various *ETp* and *ETd* values can be changed independently by tuning *Smp* and *Smd* values respectively. The amount of change in *S* also depends on the actual value of *S*, the plots are shown for a mid-value of *S* (= 1 V). The Fig. 4 shows that the change in synaptic strength is dependent both on the eligibility trace value and DA level, similar to the product in equation (2).

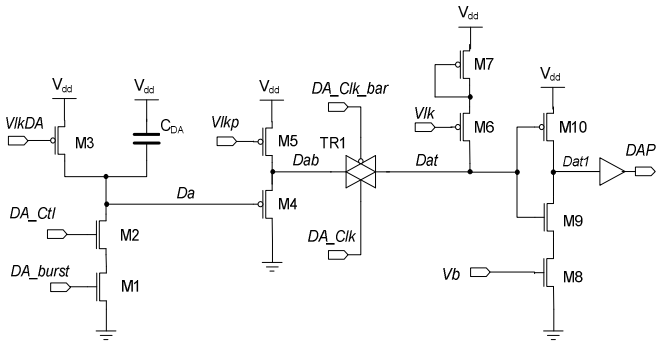

Fig. 3. DA generator circuit of DA modulated synapses.

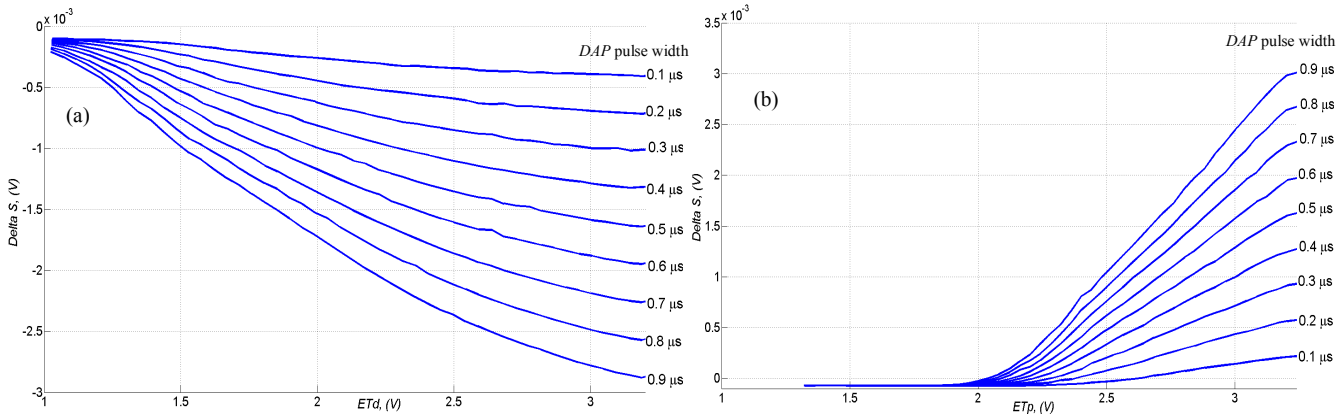

Fig. 4. Changes in synaptic strength *S* with the variation of (a) *ETd* for different *DAP* pulse widths, (b) *ETp* for different *DAP* pulse widths.

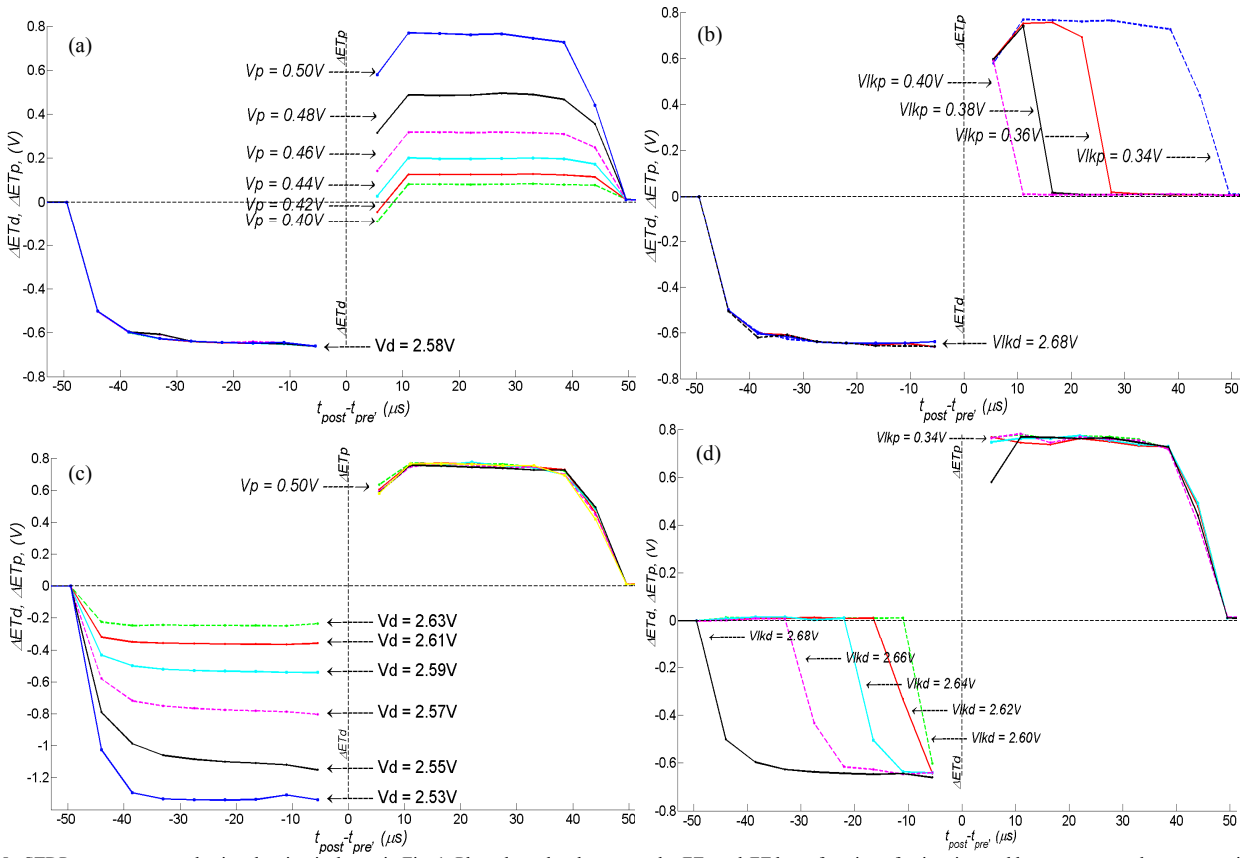

Fig. 5. STDP curves generated using the circuit shown in Fig. 1. Plots show the changes to the *ETp* and *ETd* as a function of a time interval between pre- and post-synaptic spike; *ΔETp* curves with variation of control voltages (a) *Vp*, and (b) *Vlkp*; *ΔETd* curves with variation of control voltages (c) *Vd* and (d) *Vlkd*.

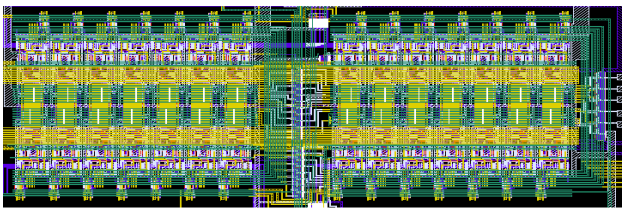

Fig. 6. Layout of the 28 DA modulated synapses and two DA generator circuits.

IV. Implementation

A test circuit containing 28 DA modulated synapses, two DA generator circuits and two cortical neuron circuits [5], has been sent for fabrication in a standard 0.35 µm CMOS technology. The layout of these circuits is shown in Fig. 6. The size of the synapse cell layout is 26 µm x 50 µm and these synapses can be configured to work as DA modulated synapse or as a STDP synapse without the DA modulation. The synapse circuit typically consumes between 2 µW and 5 µW power at *pre* and *post* synaptic spike rates of 200 kHz (i.e high neural activity level), but it could be as high as 40 µW, depending on the synapse state, parameters and spike rates. The DA generator circuit, which is shared by many synapses, consumes up to 600 µW of power (worst case).

V. Conclusions

We have presented a dopamine-modulated synapse circuit. The circuit implements a model similar to the one proposed in [4], where eligibility traces are used to provide the dynamics required to facilitate the learning of synaptic strength based on spike-time-dependent plasticity rule and a distal reward signal. The circuit has applications in VLSI implementations of biologically-plausible neural networks.

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