Integrated Circuit Implementation of a Cortical Neuron

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***Abstract*— This paper presents an analogue integrated circuit implementation of a cortical neuron model. The VLSI chip prototype has been implemented in a 0.35 µm CMOS technology. The single neuron cell has a compact layout and very low energy consumption, in the range of 9 pJ per spike. Experimental results demonstrate the capability of the circuit to generate a realistic spike shape and a variety of spiking and bursting firing patterns. The models of various cortical neuron types are obtained in a single circuit, through the adjustment of two biasing voltages, making the circuit suitable for applications in reconfigurable neuromorphic devices that implement biologically plausible spiking neural networks.**

I. INTRODUCTION

Recently, there has been an increasing research interest in developing computing architectures inspired by biology, in particular based on the models of the animal nervous system [1-7]. In addition to high-level features such as ability to perform complex pattern recognition and motor control, autonomous learning, adaptability etc. also the low-level features, such as robustness against noise and fault tolerance, make the brain-inspired system an attractive alternative computing model which could be appropriate for designing systems in contemporary and future integrated circuit technologies.

The study of the brain reveals that cortical neurons are diverse in their behaviour and many neuron types have been identified, based on electrophysiological characterisations [8-11]. Hence, in addition to the structural complexity of the network, the heterogeneity of neuronal responses and their complex non-linear oscillatory nature has made it a difficult and challenging task to build large-scale massively parallel VLSI networks that closely resemble the circuits of the cortex. While it remains an open question, at which level of abstraction neural circuits should be modeled to yield a practical computational architecture, the implementation of basic cells, capturing temporal dynamics exhibited by spiking neurons, has been a subject of on-going research interest [12-19]. Table I summarizes properties of various implementations found in the literature. Silicon area needed to implement the circuitry is an important consideration for VLSI design, and while the direct comparisons are difficult without considering implementation details, we have included transistor count as an indication of the overall circuit area requirements. The Integrate and Fire (I&F) neuron cells typically use approximately 20 transistors to implement an adaptive neuron [12] [13]. More realistic circuits, implementing conductance-based neuron models have been reported in the literature [14] [15], however, these circuits use a larger number of transistors. Several other implementations have been proposed [16-20] that are based on mathematical models that capture some of the features of the neuron's oscillatory behaviour. In [21] we have proposed a novel circuit model, which allows the implementation of a cortical neuron using only 14 transistors. The spiking shape produced by the circuit is biologically plausible, and a variety of spiking patterns such as regular spiking, fast spiking, low threshold spiking, intrinsic bursting, chattering etc. can be obtained. In this paper, we report the results obtained from the integrated circuit implementation of the proposed neuron circuit. The circuit is briefly introduced, the chip design is overviewed, and experimental results are presented and discussed.

TABLE I. REVIEW OF VLSI NEURON MODELS.

Neuron model	Approximate Number of transistors	Spiking pattern	Biological plausible spike shape	Reference
Conductance-based	27-30+	Simple spike	good	[14]
Integrate-and-fire	18-20	Simple spike	fair	[13]
FitzHugh-Nagumo	20	Oscillatory	envelope	[16]
Morris-Lecar	20	Oscillatory	envelope	[17]
Resonate-and-Fire	20	Oscillatory	pulse	[18]
Hindmarsh-Rose	90	Bursting	fair	[19]
Proposed model	***14***	***All types***	***good***	

II. THE CIRCUIT

The proposed circuit is loosely based on the Izhikevich neuron model [11], which uses two differential equations and a reset mechanism to generate the required oscillatory behaviour. In our model, we have replaced the simple mathematical equations with ones more suitable for implementation using CMOS technology, exploiting the underlying nonlinear characteristics of MOS transistors to implement the neuron using as few transistors as possible. The circuit is presented in Figure 1. The implemented neuron model consists of two state variables: "membrane potential" (V) and "slow variable" (U), that are represented by voltages across capacitors C_V and C_U respectively. The circuit comprises three functional blocks: membrane potential

circuit, slow variable circuit and comparator circuit (the transistors M1 and M2 are shared by the membrane potential and slow variable circuits). In the membrane potential circuit, the capacitor C_V integrates the postsynaptic input current, plus internal currents which depend on the state of the cell. Similarly, in the slow variable circuit the capacitor C_u integrates the currents that non-linearly depend on U and V. The comparator detects the spike and generates pulses (V_A and V_B) that perform the after-spike reset. Various spiking and bursting firing patterns are obtained by tuning two voltage parameters, V_c and V_d, which control the reset mechanism. A more detailed explanation of the circuit behaviour, circuit analysis using phase plane dynamics and mathematical equations of the model are provided in [22].

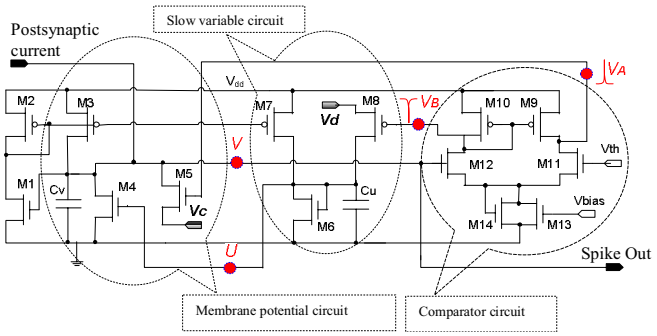

Figure 1. The compact silicon cortical neuron circuit.

III. Integrated Circuit Implementation

To experimentally verify the behaviour of our neuron cell we have designed an integrated circuit, fabricated in a 0.35µm CMOS technology. The chip contains 202 neuron cells, with varied circuit parameters (transistor sizes and capacitances) to confirm the simulation results related to transistor scaling and variability [21]. A microphotograph showing the chip layout, as well as individual cells is shown in Figure 2. The purpose of the chip was to experimentally verify the spiking behaviour of a single cell, and thus the cells are individually accessible and do not form any network. In addition to the neuron cells the chip contains required multiplexers, buffers and simple synaptic circuitry to generate excitatory and inhibitory postsynaptic currents. The different neurons are provided with three different types of output buffers to feed the membrane potential signal to the output pads, These types include single stage buffering with two nMOSFETs, double stage buffering with two nMOSFETs and operational amplifier buffering. The circuit also contains a multiplexing unit that selects one neuron at a time. Some cells are designed with an additional external membrane potential resetting circuit using a single transistor. All the experimental results presented in the following sections are taken from a single neuron cell, and its circuit parameters are: $(W/L)_{M1}$= (2.3/1), $(W/L)_{M2}$= (2.3/1), $(W/L)_{M3}$= (2.3/1), $(W/L)_{M4}$= (1.3/22), $(W/L)_{M5}$= (5.3/1), $(W/L)_{M6}$= (1.3/18), V_{th} =1.70V, $(W/L)_{M7}$ = (1.3/14), $(W/L)_{M8}$= (1.3/1), V_{dd} = 3.3V, V_{bias} = 0.6V, C_v=0.1pF, C_u=1pF .

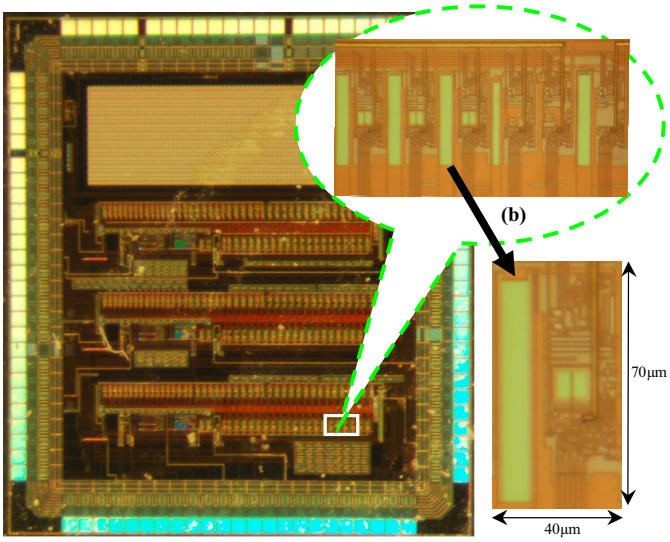

Figure 2. Photograph of the fabricated device: (a) chip with 202 neurons having different circuit parameters; (b) six different neuron cells; (c) a single neuron including an output buffer and control circuit.

IV. Experimental Results

The synaptic input was applied to the circuit using a pulse generator, and the biasing parameters were set using programmable voltage supplies. The membrane potential waveforms (buffered using on-chip operational amplifiers) were recorded using a digitising oscilloscope. Figure 3 shows different responses of the circuit to a postsynaptic input current step of 0.1µA and their respective parameters of the tuning voltages V_c and V_d are provided in Figure 4. The circuit mimics various types of cortical neuron firing patterns: *chattering*, (CH), *intrinsic bursting* (IB), *low-threshold spiking* (LTS), *fast spiking* (FS) and *regular spiking* (RS). Brief definitions of each of these firing patterns are presented in [22]. It should be noted that the circuit does not operate in biological real-time, but on approximately 10^4 faster time scale. For comparison purpose, scaled time domain is considered in order to adopt biological classifications methods given in [8]. The classification of spiking and bursting firing patterns using inter-spike interval histograms obtained from the simulations was presented in [21], frequency of spiking and the accommodation (spike frequency adaptation index) were used to further classify these neurons.

The adaptation index measures the accommodation of the firing pattern, i.e. the progressive decrease in firing frequency despite the maintained depolarization. The adaptation index is calculated as $100\times(1-F_{ad}/F_1)$, where F_1 corresponds to the firing rate of the first inter-spike interval and F_{ad} is the adapted firing rate [8]. The approximate values of delay (δt) between the start of the supra-threshold current injection and the first spike of the spike train, adaptation index and frequency of spiking values for each of RS, LTS and FS type firing patterns are provided in Table II.

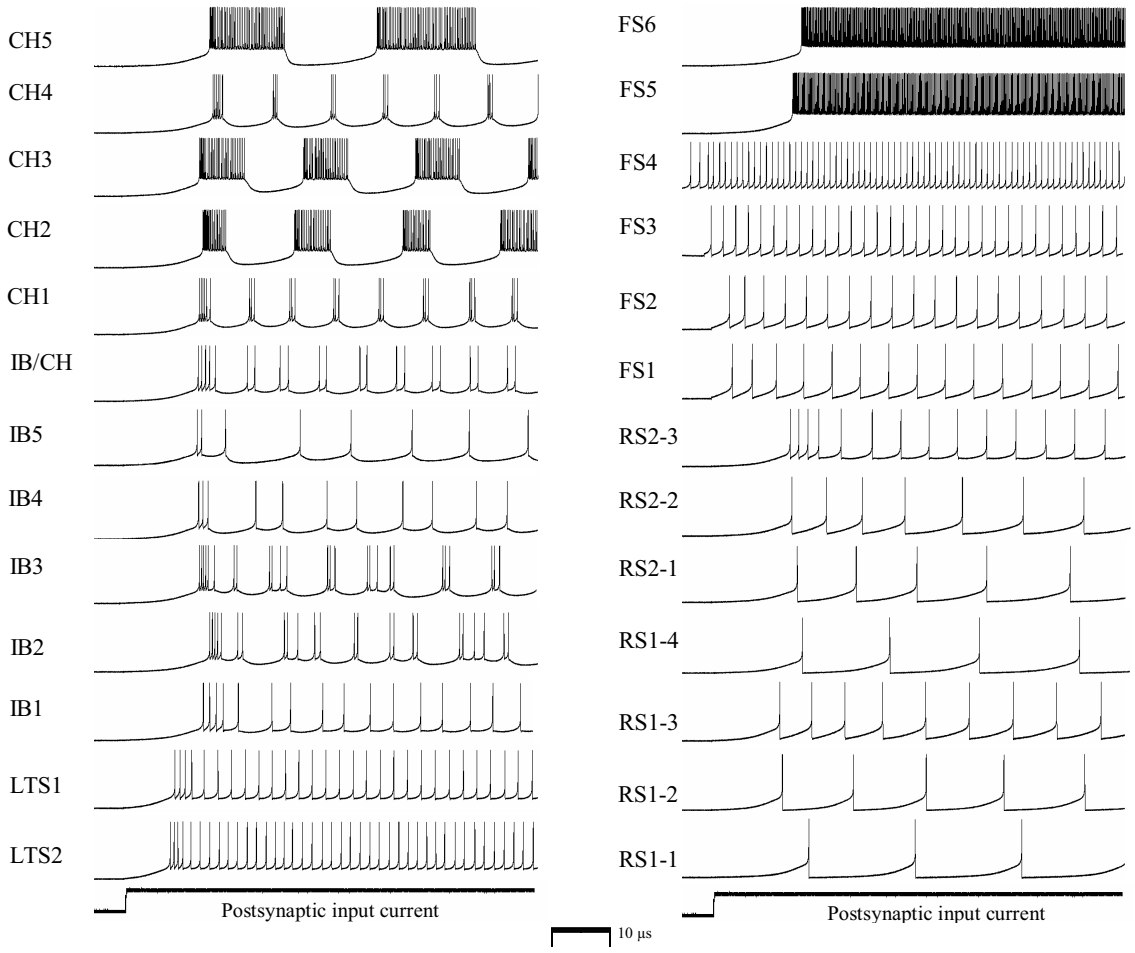

Figure 3. Experimental waveforms of CH, IB, FS, LTS RS1 and RS2 cells. Each plot shows voltage response of the fabricated circuit to a 0.1µA of step current. Parameters *Vc* and *Vd* of each response are provided in Figure 4.

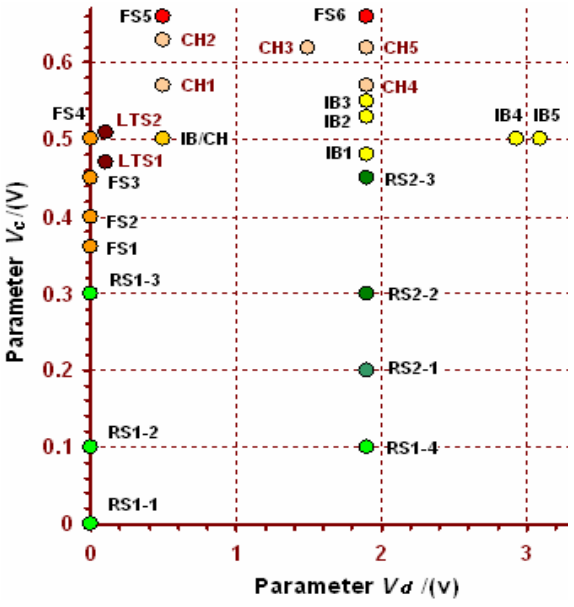

Figure 4. Parameters *Vc* and *Vd* that were used to obtain the cortical neuron firing patterns given in Figure 3.

TABLE II. NEURAL PROPERTIES OF RS, LTS AND FS FIRING PATTERNS PROVIDED IN FIGURE. 3.

Label	Delay* δt (≈ in µs)	Adaptation Index (≈ in %)	Frequency of spiking (≈ in kHz)	Type
RS1-1	17	0	50	RS-1
RS1-2	13	13	70	RS-1
RS1-3	12	24	130	RS-1
RS1-4	16	22	51	RS-1
RS2-1	15	35	65	RS-2
RS2-2	14	44	90	RS-2
RS2-3	14	72	190	RS2
LTS1	9	72	300	LTS
LTS2	8	65	480	LTS
FS1	4	21	220	FS
FS2	3	22	280	FS
FS3	1	4	400	FS
FS4	<1	2	1000	-
FS5	14	22	5500	FS
FS6	16	35	6300	FS

*Delay between the start of the supra-threshold stimuli and the initial spike

It can be seen that all the firing patterns across V_d=0V are weak-accommodating resulting in either RS1 [9] or FS type firing patterns. The FS4 type neuron continues its spiking even after the supra-threshold current is removed, however, it shuts if the inhibitory postsynaptic current is provided. The FS1, FS2, FS3 and the rest of the firing patterns where V_d=0 and 0.36V<V_c<0.5V behave as a FS type and their frequency of spiking lies in between 200 kHz to 800 kHz. In Figure 4, the approximate parameter space area where 0.2V<V_d<3.25V and V_c<0.4V results in the RS neuron type and when V_c increases from 0 to 0.4V the frequency of spiking and adaptation index values increase. The parameter space area where 0.2V<V_d<3.25V and 0.45V<V_c<0.56V results in IB type and different IB firing patterns can be obtained by varying V_d and V_c appropriately. Similarly, the area where 0.2V<V_d<3.25V and 0.56V<V_c<0.65V produces CH behaviour and various number of spikes in a burst and inter-bursting frequencies can be obtained by varying V_d and V_c. In the same V_d region when V_c is greater than 0.65V the cell produces a delayed FS firing pattern with higher firing frequency. Variations of firing patterns of the selected RS, IB, CH, and FS cell types with the variation of V_c across V_d=1.9V illustrate the sensitivity of the firing patterns and their properties to the tuning variable V_c. It is also important to note that further variations of behaviour can be obtained by changing the W/L of transistors M4, M6 and M7 [21].

Depending on the type of the firing pattern, the power consumption of a cell can vary between 0.1-60μW and is approximately proportional to the average spiking frequency. The energy per spike provides a figure of merit that allows a fair comparison of power consumption with respect to the circuit's computational performance. In our circuit the energy consumption per spike is 8.5-9.0 pJ (value obtained via post-layout simulations). For comparison, the I&F circuit described in [13] consumes 3-15 nJ/spike. The high energy efficiency of our implementation is a result of the higher operating frequency, biasing with low dc currents, and the circuit topology that minimizes the current paths that do not directly contribute to the implementation of the circuit dynamics (i.e. charging and discharging of C_u and C_V [22]). However, it has to be remembered that a complete neural system will need to include synapse models and spike communication mechanisms, which are likely to dominate the energy requirements. It can be also noted, for comparisons, that a simulation of the Izhikevich neuron [11] on a conventional digital hardware platform consumes somewhere in the range of 1 μJ per spike.

V. Conclusion

We have presented an integrated circuit implementation of a compact 14-transistor CMOS cortical neuron circuit. It has been verified experimentally that the circuit is capable of generating many types of cortical neuron behaviour, with diversity similar to that of biological neuron cells. The circuit provides a simple, compact and easily configurable universal cortical neuron, with potential applications in the development of massively parallel analogue VLSI neuromorphic chips that closely resemble the circuits of the neocortex.

Acknowledgement

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