Simple Analogue VLSI Circuit of a Cortical Neuron

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***Abstract*— This paper presents a novel analogue VLSI circuitry that reproduces spiking and bursting firing patterns of cortical neurons, using only 14 MOSFETs. The circuit provides a basic building block for the development of neuromorphic architectures. It enables implementation of many neurons in a single silicon chip while exhibiting flexibility in obtaining different types of adaptive and oscillatory neuron behaviours, by simply adjusting the biasing voltage. The simulation results, using a 0.35um CMOS technology, are presented.**

I. INTRODUCTION

There is a growing interest in spike-based neural networks using approaches inspired by neurobiology, as they appear to provide promising solutions to a variety of complex problems, some of which might be beyond the capability of most powerful computers. Hence the design and fabrication of spiking neural network VLSI circuits have attracted increasing research interest [1-7]. Among these applications, integrate and fire (I&F) neuron is widely used due to its simplicity and small size of the neuron circuitry. However, typically used I&F neuron cells consume approximately 20 transistors to implement low power adaptive neuron circuitry [8] [9]. Furthermore, I&F neurons exhibit simple spiking behaviour only; this might be not adequate for the development of truly large–scale, distributed, massively parallel networks of VLSI circuitry which would be capable of imitating the processing of human nervous system, as approximately 90% of the cortex is made of non-linear oscillatory neurons rather than simple spiking neurons. Therefore attention of some researchers has focused on implementing simple neuron circuits that are capable of providing different types of cortical spiking behaviour by utilising as few transistors as possible to enable integration of large number of cells in a single chip.

Circuits implementing conductance-based neuron models (Hodgkin-Huxley type) have been reported in the literature [10][11]. However, these circuits consume large number of transistors. The circuit implementations of oscillatory neuron models such as the FitzHugh-Nagumo neuron model [12], the Morris-Lecar neuron model [13], the Resonate-and-Fire neuron model based on the Volterra system [14], the Hindmarsh-Rose neuron model [15] and Hardware Oregonator model [16] have consumed around 20 transistors. However, all these models do not reproduce accurate shapes of the spikes generated by biological neurons and are not capable of producing different types of cortical spiking and bursting behaviours in a single circuit with tunable parameters.

In this paper we present a simple CMOS circuitry inspired by computational model proposed by Izhikevich [17]. While that model uses as simple as possible set of mathematical equations, our model exploits underlying nonlinear characteristics of MOS transistors to implement the neuron with as few circuit elements as possible. The spiking shape given by the circuit resembles that of real neurons (although it operates on a different timescale - the VLSI neuron is more than 10^5 times faster than the biological one). The circuit is also capable of exhibiting linear and non-linear responses, with spiking patterns such as regular spiking, fast spiking, low threshold spiking, intrinsic bursting, and chattering while utilising only 14 transistors.

II. VLSI NEURON CIRCUITRY

The proposed circuit is presented in Figure 1. The implemented model consists of two state variables represented by voltages across capacitors C_v and C_u, One corresponds to the "membrane potential" (V) and other corresponds to the "slow variable" (U).

These two state variables are used to obtain a variety of bursting and spiking neuron behaviours achieved by controlling two parameters V_c and V_d, i.e voltages at nodes c and d. Based on the first order approximate analysis of the proposed circuit we obtain the following equations:

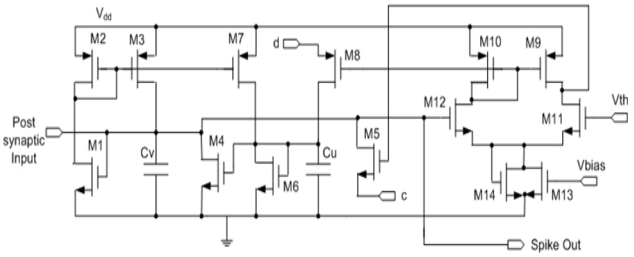

Figure 1. Proposed circuit of a cortical neuron

$$\dot{V} = \begin{cases} l_1V^2 - l_2V - l_3U^2 + l_4U + l_5 & \text{when} \quad V \geq U - V_T; \\ m_1V^2 - m_2V - m_3UV + m_4 & \text{otherwise} \end{cases}$$

$$\dot{U} = k_1V^2 - k_2V - k_3U^2 + k_4U + k_5$$

$$\text{If} \quad V \geq V_{th} \quad \text{then} \begin{cases} V \leftarrow C \\ U \leftarrow U + \Delta Q \end{cases}$$

Where, k_i, l_i, m_i, V_T, V_{th}, C and ΔQ are constants depending on transistor parameters (e.g. W/L ratio) and/or bias voltages.

The circuit comprises of 3 functional blocks, the excitatory membrane potential building and its resetting circuitry (transistors M1-M5), the slow variable building and its resetting circuitry (transistors M1, M2 and M6-M8) and the comparator circuitry (M9-M14).

The membrane potential circuit is shown in Figure 2(a). Voltage V is achieved by integration (on the capacitor C_v) of the current provided by post-synaptic input current (excitatory or inhibitory), plus the current provided by transistor M3 (which is square function of membrane potential and provides the positive feedback that generates the spiking), minus the current drawn by transistor M4 (which is related to the slow variable U, as well as V).

Once the membrane potential reaches a threshold voltage, V_{th}, the comparator generates a pulse that resets the membrane potential through the transistor M5 to a value set by voltage at node c.

The slow variable potential circuit is shown in Figure 2(b). Votage U is achieved by integration (on the capacitor C_v) of the current provided by M7 (which is square function of the membrane potential), minus the current drawn by M6 (which is a function of the slow variable potential itself).

During the membrane potential spike the comparator output generates a pulse; as a result the slow variable potential is incremented by an extra amount of charge through M8. The amount of increment is determined by the voltage at node d.

III. Experimental Results

The circuit has been simulated in SPICE using standard 0.35µm CMOS technology parameters. Various types of cortical neuron firing patterns: chattering (CH), intrinsic bursting (IB), fast spiking (FS), low threshold spiking (LTS) and regular spiking (RS) are observed by changing the values of the circuit variables V_c and V_d. Figure 3 shows different responses of the circuit to a post synaptic input current step of 0.1uA.

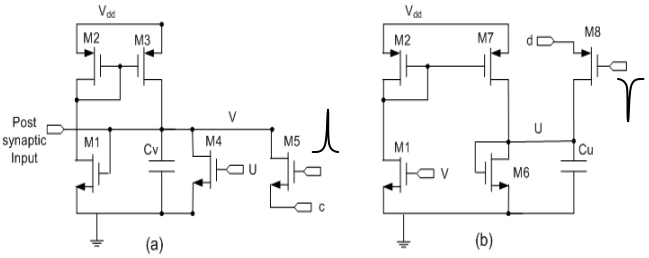

Figure 2 (a). Membrane potential circuit; (b).Slow variable circuit

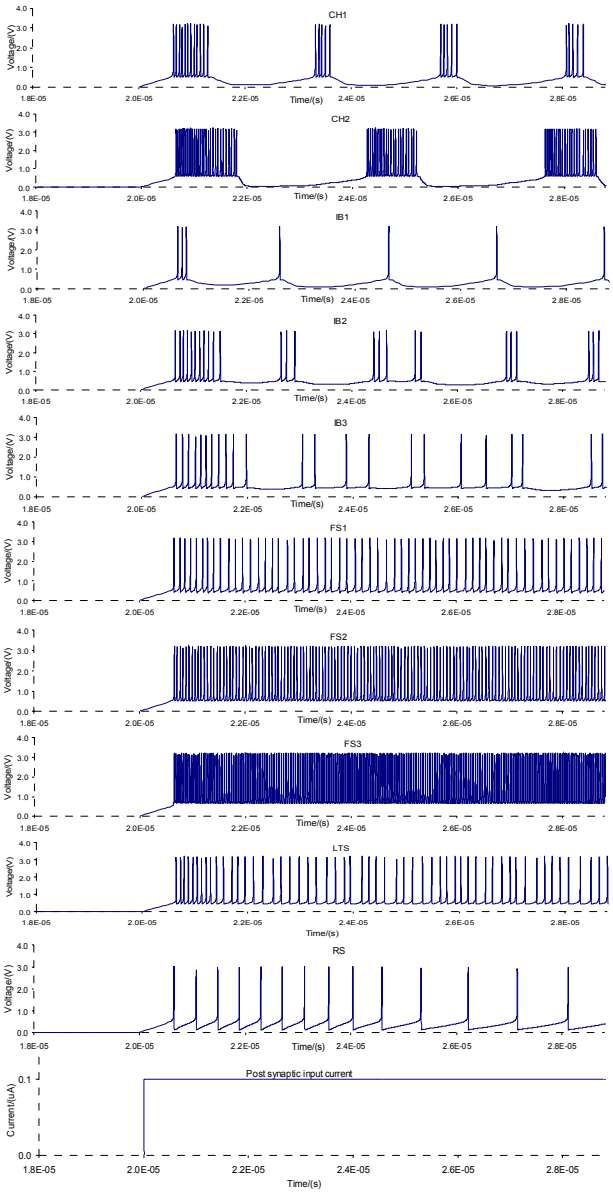

Figure 3. CH, IB, FS, LTS and RS neuron responses. Each plot shows a voltage response of the proposed circuit to a step of dc-current I = 0.1uA. Parameters V_c and V_d of each response are given in the Figure 4.

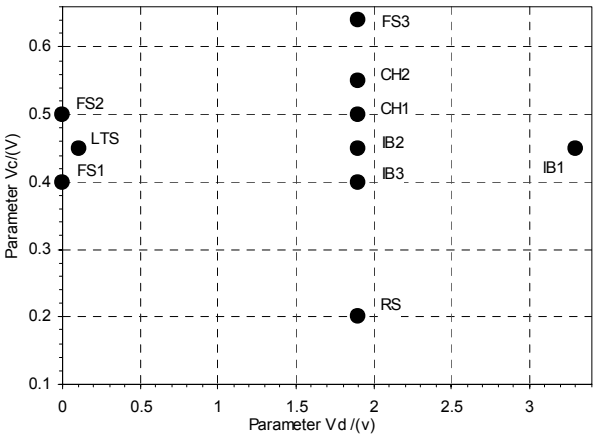

Figure 4. Values of the parameters V_c and V_d which were used to obtain cortical neuron firing patterns shown in Figure 3.

The values of tuning variables V_c and V_d used to obtain plots provided in Figure 3 are given in the parameter space shown in Figure 4. The V_c and V_d can be controlled externally and all the other variables of the circuit were kept constant and their values are $(W/L)_{M1}$= (2.3/1), $(W/L)_{M2}$= (2.3/1), $(W/L)_{M3}$= (2.3/1), $(W/L)_{M4}$= (1.3/22), $(W/L)_{M5}$= (5.3/1), $(W/L)_{M6}$= (1.3/18), V_{th} =1.70V, $(W/L)_{M7}$ = (1.3/14), $(W/L)_{M8}$= (1.3/1), V_{dd} = 3.3V, V_{bias} = 0.6V, C_v=0.1pF, C_u=1pF.

A. Characterisation of spiking behaviours

The RS neuron's frequency of spiking and the spike frequency adaptation index variation with the variation of the post synaptic input current is shown in the Figure 5. The adaptation index is quantified as $100\times(1-F_{ad}/F_1)$, where F_1 corresponds to the firing rate of the first inter-spike interval and F_{ad} is the adapted firing rate [18]. The relation between firing frequency and post synaptic current is close to linear for input currents up to 2uA. For larger post synaptic currents the firing frequency starts to saturate.

As seen in the previous section, different known types of cortical neurons have been obtained using different values of circuit parameters V_c and V_d. It is also possible to obtain each type of neuron with different characteristics, by changing the width to length ratios of the transistors M4, M6 and M7. To illustrate this, investigation of variation of fast spiking neuron characteristics with the variations of W/L of these transistors is presented in this section.

The inter spike frequency and the adaptation index variations with the variation of W/L of the transistors M6, M7 and M4 are shown in Figures 6, 7 and 8, respectively. The circuit parameters used are V_c=0.2V, V_d=1.9V and each transistor's W/L is varied in turn while keeping all the other transistor's W/L at a constant value, which was given in the previous section.

It is seen from Figure 6 that the neuron circuitry changes its characteristic smoothly when increasing the W/L of M6 and when the W/L of M6 is around 0.2 the circuit turns from RS neuron to FS neuron. It is evident that W/L of M6 can be

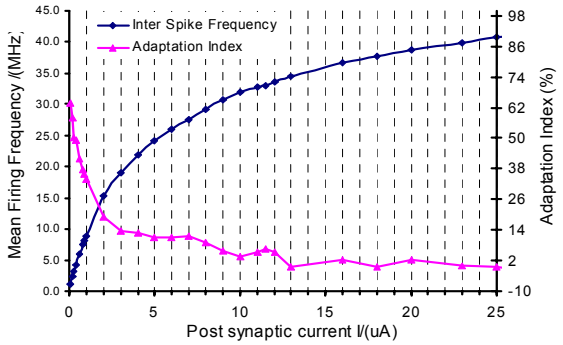

Figure 5. Variation of inter spike frequency and spike frequency adaptation index with the variation of post synaptic current of the RS neuron.

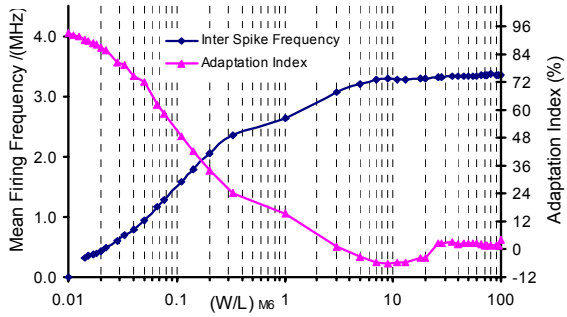

Figure 6. The variation of the inter spike frequency and adaptation index with the variation of the W/L of the transistor M6

used to obtain wide range of adaptation indices that are needed by the designer.

The spike frequency, degree of spike frequency adaptation, the spike width measurement, can be used to classify the neuron as FS or RS. The biological FS neurons tend to have higher spike frequency than the RS neurons and also typically exhibit spike frequency adaptation index value less than 35% [18]. It is clearly seen from the adaptation variation graphs (Figure 6, 7 & 8) that it is possible to design many variations of FS cells that have adaptation index less than 35% at higher frequency. The time scaling of the VLSI implementation (spike frequency in the MHz rather than Hz range) imposes a limitation upon direct comparison of spike frequency values and spike width values of the real neurons and the VLSI neurons. However it is clearly seen from the plots in Figures 6, 7 and 8 that the relative spike frequencies of FS and RS neurons implemented by the circuit are comparable with those of the biological neurons.

B. Characterisation of bursting behaviours.

Bursting and non bursting behaviours of the neurons can easily be classified using inter spike interval histograms (ISIH) as ISIHs of bursting neurons are bimodal whereas the non-bursting neurons have unimodal histograms. As illustrated by the ISIH plots in the Figure 9, spiking and bursting neurons implemented by the proposed circuit show similar response to biological neurons [18].

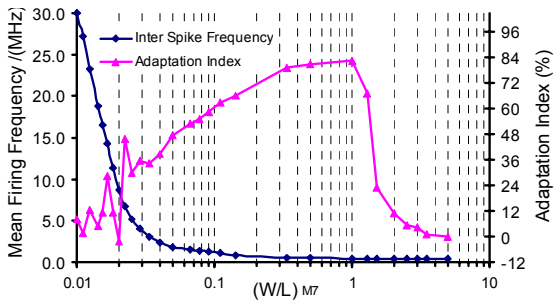

Figure 7. The variation of the inter spike frequency and adaptation index with the variation of the W/L of the transistor M7.

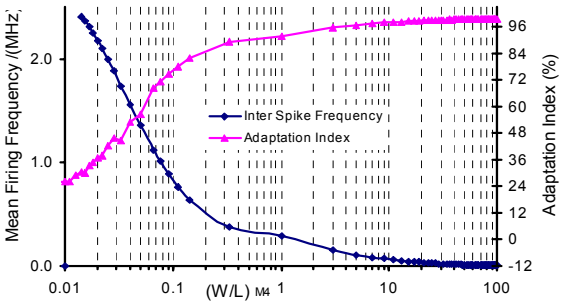

Figure 8. The variation of the inter spike frequency and adaptation index with the variation of the W/L of the transistor M4.

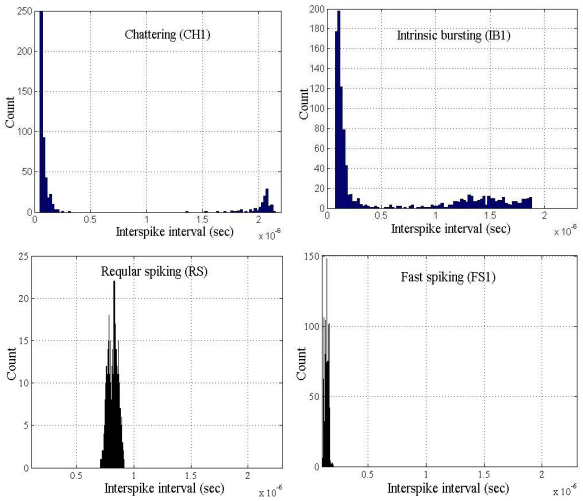

Figure 9. The inter-spike interval Histrograms of CH1,IB1,FS1 and RS firing patterns

IV. CONCLUSION

The presented CMOS circuit is designed with 14 transistors only and it provides a universal neuron cell, capable of implementing different cortical neuron types, producing spike shapes and patterns similar to those observed in electrophysiological experiments with real neurons. Apart from implementing different types of neurons, this circuit also enables the designing of a variety of different behavioural cell clusters in each cortical neuron types, with diversity similar to that of biological neuron cells. The variety of behaviour is obtained in a single circuit, only requiring changing two bias voltages. These voltages can be set externally or could be stored/controlled locally enabling dynamic switching of spiking modes and characteristics. If further flexibility is required, different characteristics could be also obtained in a single circuit by using digitally programmable switches to select W/L of the transistors.

The proposed VLSI neuron model provides a foundation for designing analogue neuromorphic VLSI circuits closely resembling the circuits of the cortex, enabling the design of systems that can adapt and learn, imitating the processing of human brain.

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