A CMOS circuit implementation of a spiking neuron with bursting and adaptation on a biological timescale

Jayawan H. B. Wijekoon and Piotr Dudek
School of Electrical and Electronic Engineering,
The University of Manchester,
United Kingdom.

Abstract— **This paper proposes a silicon neuron circuit which uses a slow-variable controlled leakage term to extend the repertoire of spiking patterns achievable in an integrate and fire model. The simulations reveal the potential of the circuit to provide a wide variety of neuron firing patterns observed in neocortex, including adapting and non-adapting, regular spiking, fast spiking, bursting, chattering, etc. The firing patterns of basic cell classes are obtained with a simple adjustment of four biasing voltages. The circuit operates in the sub-threshold regime, with time constants similar to biological neurons, and hence is suitable for use in systems requiring such operating speeds. Envisaged applications of the proposed circuit are in large-scale analogue VLSI systems for spiking neural network simulations, brain-inspired circuits for robotics and hybrid silicon/biology systems.**

I. INTRODUCTION

Since the pioneering work of Mead [1] on "neuromorphic" circuits, there has been a continuing interest in developing electronic devices that mimic the operation of biological brains. In particular CMOS implementations of 'silicon neurons' have been a subject of on-going development [2-6]. Recently, a number of systems have been proposed [7-9], that attempt to integrate thousands of silicon neurons in a single chip. In some cases (e.g. [9]), these silicon neurons are operating at speeds far exceeding those of biological neurons, and are intended to provide a computationally powerful simulation acceleration tool. This is motivated by the relative ease with which electronic circuits can operate at frequencies far exceeding these typically observed in biological neural systems (e.g. typical mean firing frequencies of neurons in the cortex are in the order of 10 Hz and the time courses of membrane potentials have bandwidth limited to several kHz). However, the technological constraints of the common communication infrastructure used for neuromorphic hardware, i.e. the address event representation (AER) framework, as well as the desire to interface directly to sensors that operate on signals encountered in nature and timescales similar to biology, lead to the situation where the majority of silicon neurons proposed in the literature have been designed to operate in biological real-time (in this context, 'real-time' means the operational speed equal to that of the system these circuits are trying to emulate, i.e. biological neurons). Amongst these devices, several neuron models have been considered as a basis for circuit implementation, from integrate-and-fire (I&F) neurons [4], to non-linear conductance-based [7,8] and Hodgking-Huxley like [5,10] models. The latter are of particular interest, as they exhibit much richer dynamics and thus possible repertoire of spiking behaviours, both in the context of the network and individual responses to a fixed stimulus.

In our earlier work [11] we proposed a neuron circuit that operated on accelerated time scale (10^4 times faster than biological neurons). The circuit was inspired by the computational model proposed by Izhikevich [12] and motivated by the desire to achieve, in a single, easily tuneable circuit, a variety of action potential shapes and activity patterns that are encountered in mammalian cortex, whose neurons exhibit a variety of spiking adapting, non-adapting, and more complex bursting firing patterns [16]. That circuit made use of the quadratic relationship in a saturated MOS transistor. To operate on a biological time scale, however, large capacitors and long transistors would be required. In this paper we present a circuit that can be used with sub-threshold currents, to achieve spiking/bursting neuron with real-time operation in a compact circuit.

The rich dynamic behaviour of the Izhikevich [12] model is produced in a system of two differential equations describing the evolution of a 'membrane potential' variable (V) and a 'slow' variable (U), together with an after-spike reset mechanism. It should be noted that this reset mechanism is more similar to the reset in the I&F model than a spike generating mechanism of biological sodium/potassium channels. However, the rich repertoire of behaviours, including adaptation and bursting, is a result of the dynamics of V and U, which can be qualitatively associated with the interplay between faster sodium/potassium dynamics and slower calcium dynamics. A similar mechanism for adaptation and bursting is also present in the exponential I&F model Brette and Gerstner [13]. A linear I&F model can also been extended to enable adapting and bursting behaviours, via mechanisms such as variable thresholds in Gerstner's spike response model [14], and some additional dynamic variables such as "burst currents" proposed by Michalas and Niebur [15].

This work has been supported by the EPSRC, grant number EP/C010841.

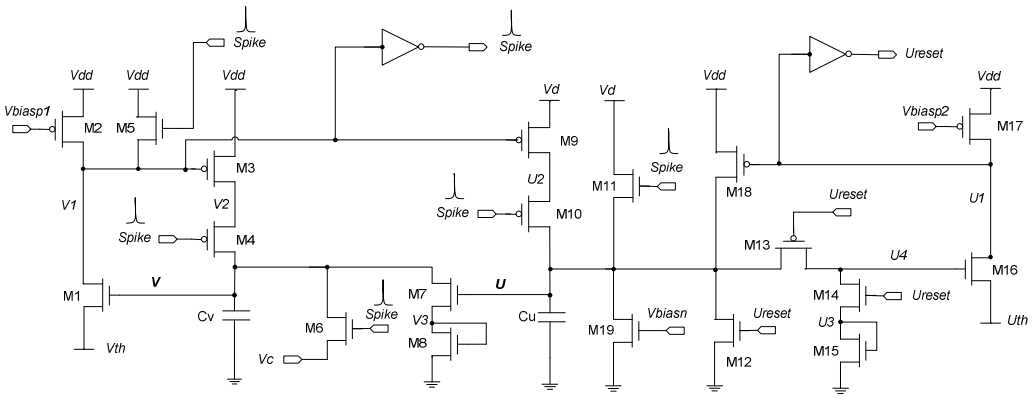

Figure 1. Proposed cortical neuron circuit

Here, we propose a circuit that combines the simplicity of the I&F model with the slow-fast variable interactions present in the Izhikevich model. As a result, we obtain a large variety of spiking behaviours in a simple circuit, with fixed thresholds, and only two dynamic variables (V and U). The circuit can be configured to produce spiking patterns of cortical neurons, including regular spiking (RS), fast spiking (FS), low threshold spiking (LTS), chattering (CH), intrinsic bursting (IB) and thalamo-cortical (TC) neurons.

II. The Circuit

The proposed neuron circuit is shown in Figure 1. The circuit uses four tuning parameters (bias voltages U_{th}, V_{biasn}, V_c, and V_d) to configure the circuit to operate as one of the neuron types. Node voltages at V and U represent the membrane potential and the slow variable, and the currents feeding into these nodes are integrated on capacitors C_V and C_U respectively. The currents are provided by two functional circuit blocks: membrane potential circuit (transistors M1 to M8) and slow variable circuit (transistors M9 to M18).

The evolution of the membrane potential V is due to an integration, on the capacitor C_V, of the post-synaptic current (which is assumed to be injected into that node through the synapse circuit) with an exponential leakage current (generated via M7 and M8) which is determined by the value of the slow variable U. The spike threshold of V is determined by voltage Vth, and detected by M1, M2 and an inverter. M3-M5 help to control the duration of the spike and the reset dynamics. Initially M3 provides a positive feedback to quickly exceed the membrane potential threshold. The M1-M3 circuit could be also seen as providing the nonlinear feedback current similar to one present in the exponential I&F model. As a spike is generated, the feedback current is turned off by opening M4, so that the voltage at node V does not actually produce a significant voltage spike. Transistor M5 limits the output spike pulse duration, while membrane potential V is reset to the value of Vc via M6.

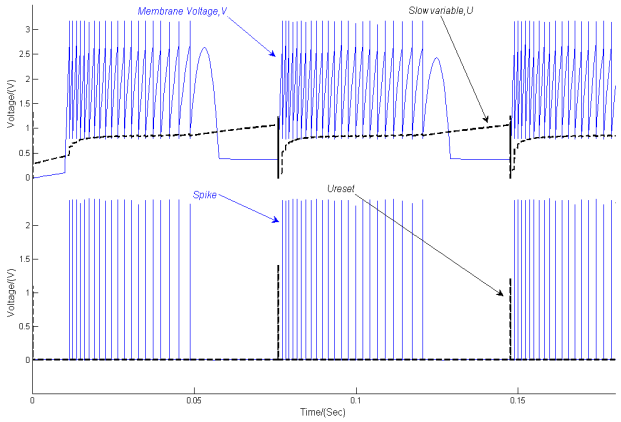

Figure 2. Waveforms of a typical CH firing pattern obtained from the circuit shown in Figure 1; top: membrane potential, V, and slow variable, U; bottom: output spikes and slow variable reset signal

As can be seen in Figure 2, the slow variable voltage U evolves at a much slower rate than the membrane voltage. The changes to the slow variable are primarily due to two reset mechanisms. After the spike is generated the value of U is pulled some amount towards V_d via M11. Additionally, when U reaches a threshold value, determined by the tuneable voltage U_{th}, a *Ureset* signal is generated (M16, M17 and the inverter) and U is reset to ground via M12. It should be noted that this reset mechanism is a novel feature of our model, and the U variable dynamics differ from the ones proposed in [12, 13]. The arrangement of M13-M15 and M18 helps to control the timings in the reset circuit. Initially, M18 provides a positive feedback to quickly bring U above the threshold value. As a result the reset signal *Ureset* goes high. Since U evolves with very slow rates, the *Ureset* is generated using a slightly different topology than the spike generation circuit. By breaking the loop using M13 switch, the *Ureset* pulse can be generated, minimising the risk of settling on to a fixed DC value in the feedback loop. The *Ureset* signal is then used to reset U to zero via M12. Finally the *Ureset* pulse is brought back to zero after the voltage at node $U4$ is brought down through M14-M15. In addition to the two reset mechanisms, U continuously evolves as two currents are integrated on capacitor C_U, one is the current through M9, which depends on the membrane potential V (M10 is used to prevent large current flow during the spike), the second one is a leakage current, controlled by V_{biasn} (M19).

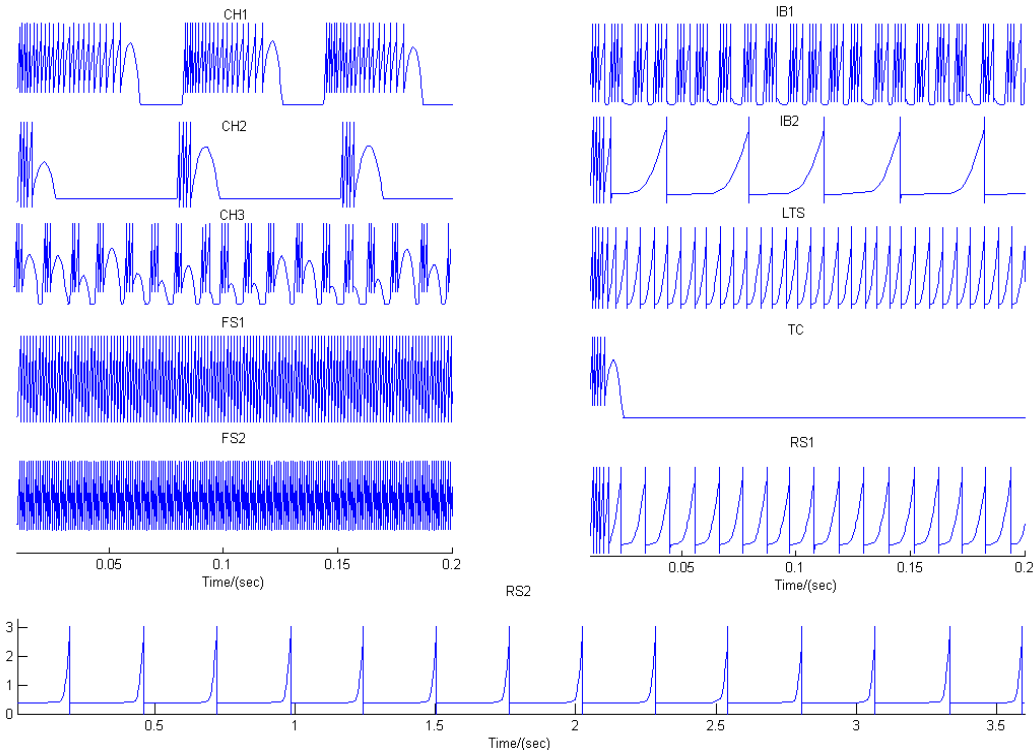

Figure 3. Membrane potential of the neural firing behaviours obtained from the neuron circuit in response to a step post-synaptic stimulus of 2nA.

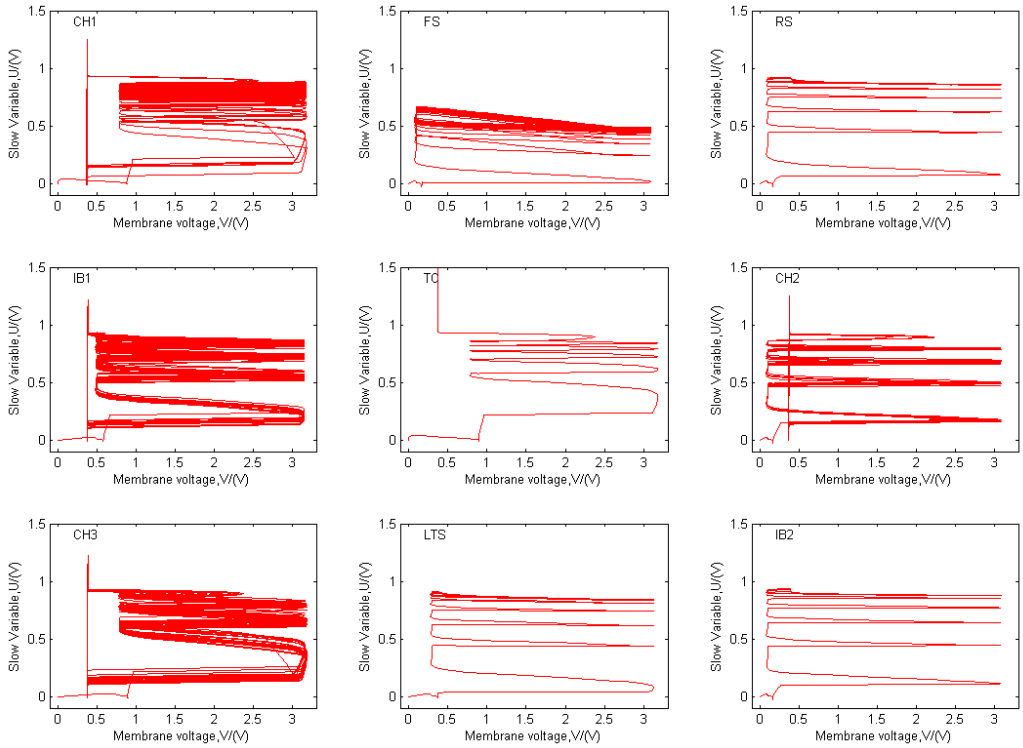

Figure 4. State trajectories of CH, IB, FS, TC, LTS & RS cells when a 2nA of postsynaptic current step is injected. (The plots are drawn using data obtained from SPICE simulations)

TABLE I. VALUES OF THE TUNING VOLTAGES USED TO OBTAIN THE FIRING PATTERNS SHOWN IN FIGURE 4

Neuron Type	Tuning Parameter/(V)			
	Uth	*Vbiasn*	*Vc*	*Vd*
CH1	0.2	0.1	0.8	0.8
CH2	0.2	0.2	0.1	1.7
CH3	0.1	0.15	0.8	1.7
FS1	0.5	0.3	0.1	1.7
FS2	1.3	0.6	0.8	1.7
IB1	0.1	0.15	0.5	1.7
IB2	0.5	0.22	0.1	1.7
LTS	0.5	0.24	0.3	1.7
TC	2	0	0.8	0.9
RS1	0.5	0.22	0.1	1.7
RS2	1.3	0.221	0	2.5

III. SIMULATION

The circuit has been designed and simulated in a 0.35µm CMOS technology. The SPICE simulation results shown in Figure 4 illustrate membrane potential *V* during various types of cortical neuron firing patterns (CH, RS, IB, FS, LTS and TC). The spike pattern classification follows methods given in [16]. The output spikes are produced at the times of membrane potential peaks. Figure 4 shows the trajectories in the state space corresponding to these firing patters. The four tuning voltage parameter values corresponding to the firing patterns are provided in Table I.

As can be seen in Figure 3, the firing patterns obtained from the proposed circuit are in the same time scale as that of the biological neurons, the minimum refractory period is approximately 1ms. The frequency of firing for a given step of post-synaptic stimulus typically ranges from below 1 Hz to 1 kHz and can be approximately configured to a desired frequency, by simply tuning the neuron using an appropriate parameter set. All the waveforms in Figure 3 are obtained using a post-synaptic stimulus of 2nA. It is observed that RS type neuron's inter-spike frequency can be configured to a one of typical RS inter-spike frequencies [16] and RS1 and RS2 sample waveforms are shown with 25Hz and 100Hz inter-spike frequencies. Similarly, the FS type neuron's inter-spike frequency can be configured to a frequency in the typical FS frequency range [16] and two selected samples (FS1 and FS2) with different inter-spike frequencies are shown in Figure 3. The proposed neuron circuit can also be configured to obtain accommodating (spike frequency adaptation) or to a non-accommodation firing pattern. In CH type firing pattern, the inter-burst interval as well as number of spikes per burst can be configured easily as seen in CH1, CH2, and CH3 waveforms in Figure 3.

IV. CONCLUSION

We have presented a silicon neuron circuit that can replicate many known types of spiking neural behaviours. It is configured by adjusting four external voltages. The circuit measures below 70um x 70um in a 0.35um CMOS technology (layout plot is shown in Figure 5). It provides a much richer repertoire of spiking patterns than a simple integrate and fire model, while using only one additional state variable. It operates with sub-threshold currents and on the same time scale as biological neurons. This configurable VLSI cortical neuron can be used for building massively parallel analogue neuromorphic networks that closely resemble the circuits of the neocortex, or in the context of interfacing electronic neural circuits with biological systems.

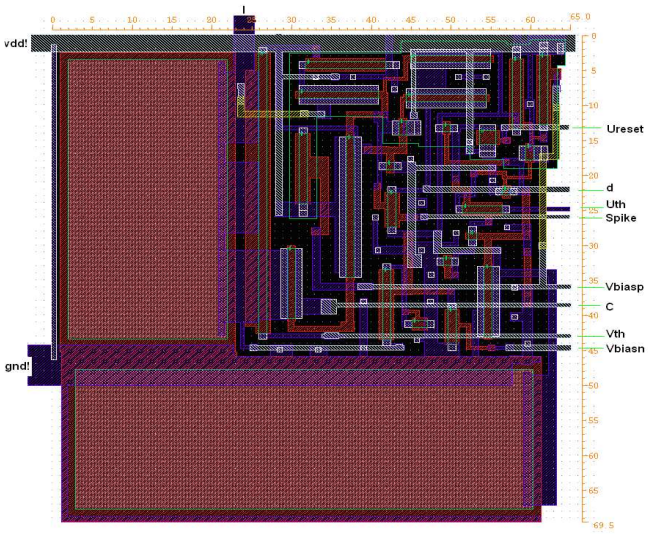

Figure 5. A layout of the proposed VLSI neuron circuit in a 0.35um CMOS technology.

REFERENCES

[1] C. A. Mead, Analog VLSI and Neural Systems, Addison-Wesley, Reading, MA, 1989

[2] Mahowald, M. and Douglas, R., A silicon neuron, Nature, 354, 1991

[3] L.S. Smith, Implementing Neural Models in Silicon, in Handbook of Nature-Inspired and Innovative Computing: Integrating Classical Models with Emerging Technologies, pp 433-475, Springer, 2006

[4] G.Indiveri, E.Chicca and R.Douglas, A VLSI array of low-power spiking neurons and bistable synapses with spike–timing dependent plasticity , IEEE Transactions on Neural Nets, 17:(1) pp. 211-221, 2006

[5] Q.Zou et.al., Real-time simulations of networks of Hodgkin–Huxley neurons using analog circuits, Neurocomputing, Volume 69, Issues 10-12, Pages 1137-1140, June 2006

[6] F. Folowosele et.al. A Switched Capacitor Implementation of the Generalized Linear Integrate-And-Fire Neuron, ISCAS 2009

[7] J.V.Arthur and K.A.Boahen, Synchrony in Silicon: The Gamma Rhythm, IEEE Trans. on Neural Nets. vol.18, no.6, pp1815-1825, 2007

[8] R.Vogelstein et.al. Dynamically Reconfigurable Silicon Array of Spiking Neurons With Conductance-Based Synapses, IEEE Transactions on Neural Networks, 18:(1), 2007

[9] J. Schemmel, J. Fieres, K. Meier: Wafer-scale integration of analog neural networks, IJCNN 2008: 431-438

[10] Farquhar, E. Hasler, P., A bio-physically inspired silicon neuron, "IEEE Transactions on Circuits and Systems", 52:(3), 477-488, 2005

[11] J.H.B.Wijekoon and P.Dudek, "Compact Silicon Neuron Circuit with Spiking and Bursting Behaviour", Neural Networks, Vol 21, Number 2-3, pp 524-534, March/April 2008

[12] Izhikevich E.M., Simple model of spiking neurons, IEEE Transactions On Neural Networks, 14:1569-1572, 2003

[13] Brette R. and Gerstner W., Adaptive Exponential Integrate-and-Fire Model as an Effective Description of Neuronal Activity, Journal of Neurophysiology, vol 94, pp. 3637-3642, 2005

[14] Gerstner W. and Kistler W.M. (2002), Spiking Neuron Models - Single Neurons, Populations, Plasticity, Cambridge Univ. Press

[15] S.Mihalas and E.Niebur, A generalized linear integrate-and-fire neural model produces diverse spiking behaviors, Neural Computation 2009;21(3):704-18

[16] L. G. Nowak et al., "Electrophysiological classes of cat primary visual cortical neurons …",J Neurophysiol,vol. 89, pp.1541-1566, Mar 2003