A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line

Piotr Dudek, *Student Member, IEEE,* Stanislaw Szczepański, and John V. Hatfield

***Abstract*—This paper describes a CMOS time-to-digital converter (TDC) integrated circuit utilizing tapped delay lines. A technique that allows the achievement of high resolution with low dead-time is presented. The technique is based on a Vernier delay line (VDL) used in conjunction with an asynchronous read-out circuitry. A delay-locked loop (DLL) is used to stabilize the resolution against process variations and ambient conditions. A test circuit fabricated in a standard 0.7-μm digital CMOS process is presented. The TDC contains 128 delay stages and achieves 30-ps resolution, stabilized by the DLL, with the accuracy exceeding ±1 LSB. Test results show that even higher resolutions can be achieved using the VDL method, and resolutions down to 5 ps are demonstrated to be obtainable.**

***Index Terms*—Delay-locked loop, time of flight, time-to-digital converter, Vernier delay line.**

I. Introduction

HIGH-resolution time-to-digital converters (TDC's) have application in a number of measurement systems, e.g., time-of-flight (TOF) particle detectors, laser range finders, and logic analyzers. Modern TOF spectrometry systems, used in particle physics experiments as well as in industrial methods of material surface analysis [1], require a TDC to have a resolution well below 1 ns, low dead-time (i.e., the minimum time between two measurements) and a large dynamic range (i.e., the maximum time interval that can be measured).

Diverse methods of digitizing short time intervals have been proposed. They include utilization of fast counters [2], analog methods based on generating a voltage ramp [3], and various CMOS tapped delay line configurations [4]–[9]. The delay line method is of particular interest, since unlike the other methods, it requires nothing more than a standard digital CMOS process. This has the advantages of relatively small cost, low power dissipation, and high integration level. A high resolution is obtained by utilizing a logic buffer delay as a time unit, and a delay-locked loop (DLL) is used to stabilize the value of the buffer delay against process variations, temperature, and power supply changes. Because the system must be designed to work properly in a "worst case," the resolution of a TDC based on a single delay line, obtainable in contemporary CMOS processes, is limited to a few hundred picoseconds.

The improvement of the resolution can be achieved by using a Vernier method [4]. In a Vernier delay line (VDL) two delay buffer chains are used. The basic configuration is depicted in Fig. 1. The measured time difference is represented by START and STOP signals (i.e., by the delay between their rising edges). The technique is based on a Vernier principle. The delay of a buffer in the upper delay chain t_1 is slightly greater than the delay of a buffer in the lower delay chain t_2. As the START and STOP signals propagate in their respective delay chains, the time difference between the START and the STOP pulse is decreased in each Vernier stage by $t_R = (t_1 - t_2)$. The position n_X in the delay line, at which the STOP signal catches up with the START signal, gives information about the measured time t_X with t_R resolution

$$n_X \cdot t_R < t_X < (n_X + 1) \cdot t_R. \tag{1}$$

In each stage, START and STOP signals are fed into an arbiter circuit (a D-type latch can perform this function) that decides which of the two input signals came first. The measured time is encoded as a position of a HI/LO transition in an output word. Since t_R is equal to a difference between the delays of two buffers, it can be made very small, and in principle, any resolution can be achieved. In practice, the time resolution will be limited by error factors, such as mismatch of the transistors and noise, and by the physical length of the delay line. Circuits with resolution down to 25 ps have been reported [7].

Other methods of improving the resolution of a delay line method, based on the difference of buffer delays, include a pulse-shrinking delay line [4] and an array of delay lines [6]. However, the pulse-shrinking delay line has an inherent burden of a long dead-time, allowing essentially only one STOP signal per measurement, and it is therefore not particularly suitable for applications where many STOP signals are generated, which is often the case (for example, in TOF particle detectors). The array method, on the other hand, makes it necessary to build very large arrays if we want to achieve significant resolution improvements. Furthermore, the extension of the dynamic range is somewhat difficult. These limitations are not present in the VDL technique.

This paper demonstrates how a high-resolution, large dynamic range, low dead-time TDC can be built using the VDL. A DLL scheme is adopted for a Vernier line to enable large dynamic range and to provide automatic calibration. A novel asynchronous read-out architecture that allows the continuous operation of the TDC with minimum dead-time is also presented.

Manuscript received July 14, 1999; revised October 15, 1999. This work was supported by the Science and Engineering Research Council (now EPSRC) of the U.K.

P. Dudek and J. V. Hatfield are with the Department of Electrical Engineering and Electronics, University of Manchester Institute of Science and Technology, Manchester M60 1QD, U.K. (e-mail: pdudek@sn1.ee.umist.ac.uk; j.hatfield@umist.ac.uk).

S. Szczepański is with the Faculty of Electronics, Telecommunications and Informatics, Technical University of Gdańsk, 80-952 Gdańsk, Poland (e-mail:stanisla@sunrise.pg.gda.pl).

Publisher Item Identifier S 0018-9200(00)00944-6.

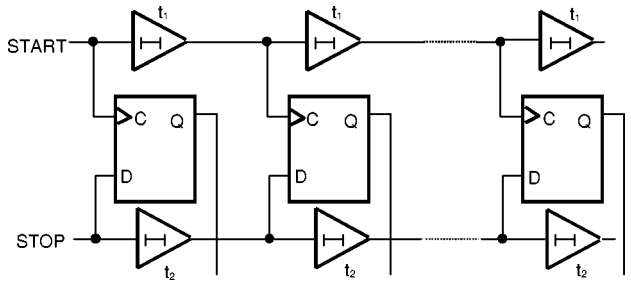


Fig. 1. VDL configuration.

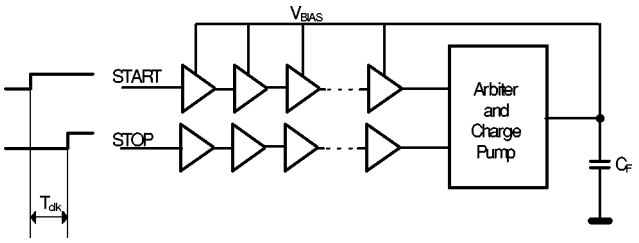


Fig. 2. DLL stabilizing difference in delays.

II. Design Issues

The dynamic range of the VDL, i.e., the maximum time that can be measured, is limited to $t_{\mathrm{DR}} = N \cdot t_R$ where N is the number of delay elements of the delay line. However, the range of the TDC can be extended by introduction of a simple counter. If we introduce a clock signal with the period T_{clk} equal to the value of the dynamic range of the VDL, then the counter, incremented on every clock cycle, will give the coarse timing information with the resolution of T_{clk} and the dynamic range limited only by the depth of the counter. The VDL will give the fine timing information, resolving the time differences between clock pulses and STOP signals.

A. DLL

The best way to ensure that $T_{\mathrm{clk}} = t_{\mathrm{DR}}$ is to lock the value of t_{DR} to the clock period by means of a DLL [10]. This will stabilize the value of t_R against temperature or power supply voltage changes and will also provide calibration against process variations. This stabilization is enabled by using voltage-controlled delay buffers in the VDL. The delay of the buffer in the upper delay chain t_1 depends on the value of a control voltage V_{BIAS}. The delay of the buffer in the lower delay chain t_2 depends only on the process and ambient conditions. The control voltage V_{BIAS} is adjusted by a feedback loop, which includes the VDL, an arbiter circuit, a charge pump, and a filter capacitor C_F, as illustrated in Fig. 2. Two pulses from a reference time base are applied to the inputs of the VDL. The delay between them is equal to T_{clk}. These pulses propagate in their respective delay buffer chains. If a delay line is N buffers long, then at the end of the line, one of them is delayed by $N \cdot t_1$ and the other by $N \cdot t_2 + T_{\mathrm{clk}}$. The arbiter circuit decides which of the pulses appears first at the output of the VDL and accordingly forces the charge pump to add charge to or remove charge from the filter capacitor, thereby changing the V_{BIAS} voltage, so that in locked mode the reference pulses appear virtually at the same time at the output of the VDL. Hence, we obtain

$$N \cdot t_1 - N \cdot t_2 = T_{\mathrm{clk}} \tag{2}$$

and therefore, the TDC resolution is made equal to

$$t_R = t_1 - t_2 = T_{\mathrm{clk}}/N. \tag{3}$$

The value of t_R is stabilized against ambient conditions and is set by a reference clock. Therefore, the fine timing information given by the VDL will have a dynamic range equal to the reference clock period. The dynamic range of the TDC can now be extended by using a coarse counter.

B. Read-Out Pipeline

Although the introduction of the coarse counter is very straightforward in the single delay line system, it is not so simple in the VDL system. This is because unlike the single delay line, the resolving time of the VDL (i.e., the time after which the complete timing information is latched in the delay line registers) is larger than the dynamic range of the line. The resolving time t_{RES} is the time of propagation of the START signal in the delay line and is equal to $t_{\mathrm{RES}} = N \cdot t_1$. Since the delay of a buffer t_1 is greater than a time resolution t_R, we obtain $t_{\mathrm{RES}} > t_{\mathrm{DR}}$. This means that the next clock pulse starts to propagate in the delay line while the previous one is still propagating. If we also want to enable multiple STOP pulses propagating at the same time in the delay line, it leads to the situation, where there is no single moment in time, when the outputs of all delay line latches could be read. The authors proposed a solution to this problem in [11], which is briefly recalled here.

The problem of reading-out the information from the VDL is solved by an introduction of an asynchronous pipelined read-out scheme as depicted in Fig. 3. The VDL is divided into k_S sections. Each section comprises N_S delay stages and works as an "independent" VDL. It is effectively resolving STOP signals that come in a certain time-window of a global clock period. At the output of each section, CLOCK (which works as a START signal) and STOP pulses are skewed by the time $N_S \cdot t_R$, which is the width of the time-window.

Because the propagation time through the section is equal to $1/k_S$ of the propagation time through the whole VDL, it can be ensured that all the delay line latches of one section are latched at some instant. At this instant, the outputs are latched into pipeline registers. If we use level-sensitive latches, we have to ensure that the worst-case CLOCK signal delay through the section is smaller than a half of the clock period (with a suitable margin for setup of the latches, etc.). Therefore, as a general guideline, it must be observed that in all conditions

$$t_1/t_R \cdot k_S < \frac{1}{2}. \tag{4}$$

This can be easily achieved by appropriate dimensioning of the transistors and by choosing adequate section lengths.

The sections are clocked by delayed clocks, and if (4) is observed, it is also ensured that when the results from one section are latched, the pipeline registers from the previous section still contain the timing information from the previous time-window

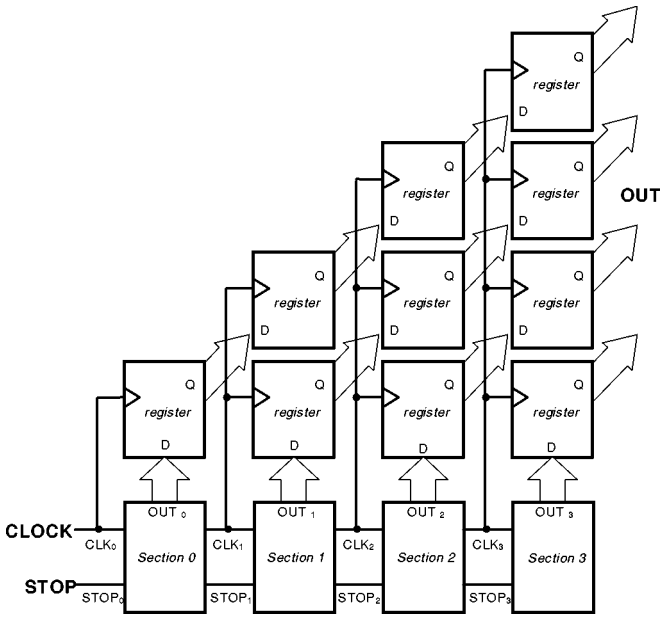


Fig. 3. Read-out scheme. The system with $k_S = 4$ sections is shown.

of the same clock cycle. The information is passed through the pipeline as the CLOCK signal travels along the delay line. In this way, at the output of the register pipeline, there is a full timing information about the STOP pulses in one clock cycle, and this information is updated on every clock cycle. Therefore, the TDC can be operated continuously, without dead-time. Coarse counter data can be then easily appended. The performance of this read-out scheme has been confirmed through simulation.

III. Implementation

To evaluate the performance of the VDL, we have designed an integrated circuit that was fabricated in 0.7-μm digital CMOS technology. The chip architecture is presented in Fig. 4. It consists of two VDL's (one for measurements and one for the DLL), complete DLL circuitry, and a simplified parallel-input/serial-output read-out circuitry. Delay lines are $N = 128$ buffers long. The chip microphotograph is presented in Fig. 5. Total chip area is 3.2 mm $\times$ 3.1 mm.

As a voltage-controlled delay buffer, the circuit shown in Fig. 6 was used [5]. Voltage-control of the delay is obtained by introducing current starving transistors M3 and M4 into CMOS inverter circuits. It has to be ensured, by careful design and simulations for extreme cases, that for any process and ambient conditions, the desired value of t_R can be achieved for some V_{BIAS} value. It is also very important, in order to prevent the signals from disappearing during propagation in the delay line, to ensure that rising and falling edges are equally delayed. Therefore, complete symmetry of the two inverter stages of the delay buffer must be preserved in the layout. We achieved this by introduction of "dummy" devices where necessary to make sure that parasitic capacitances are as well matched as possible. The measured delay versus voltage characteristic of the voltage-controlled buffer is presented in Fig. 7.

The accuracy of the time-to-digital conversion depends on the matching of the buffer delays. The delay depends on the values

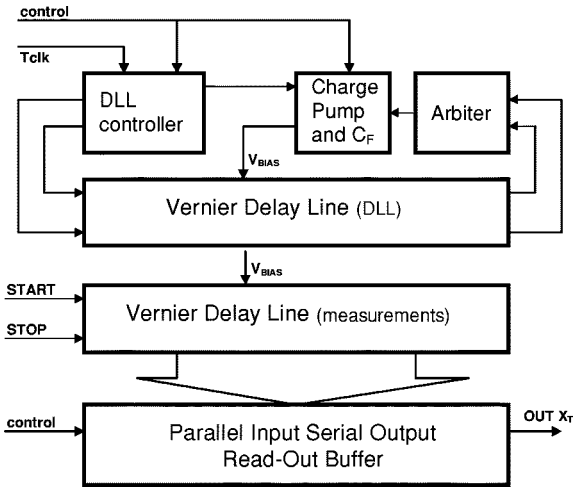


Fig. 4. The TDC chip architecture.

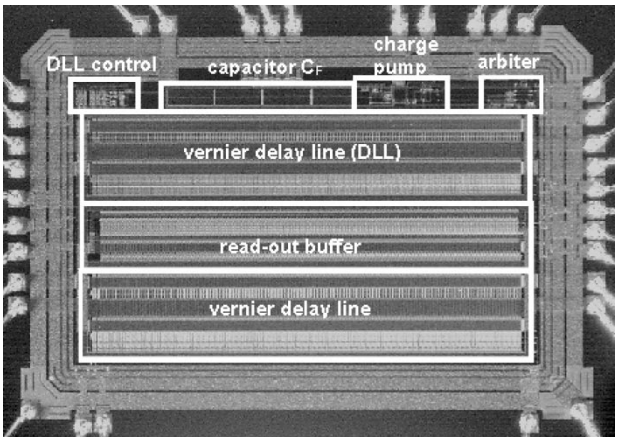


Fig. 5. The die microphotograph.

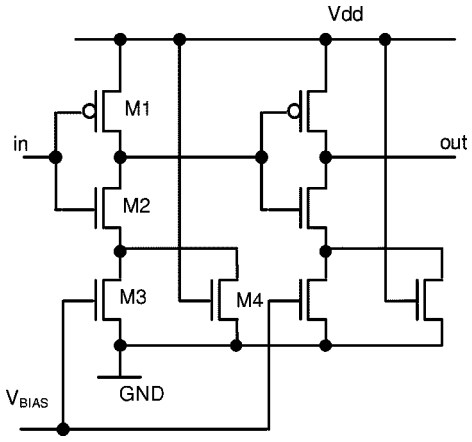


Fig. 6. Voltage-controlled buffer.

of the currents in the MOS transistors and the values of various capacitances, which are mostly parasitic transistor capacitances. Therefore, overall accuracy will be limited by mismatch of identically laid-out MOS transistors. Since mismatch is caused by local fluctuations of some physical properties which get averaged over larger areas [12], relatively large transistors should be used to achieve high accuracy. Transistor dimensions used in the present design are presented in Table I.

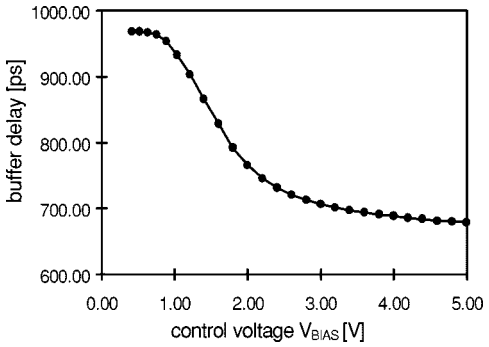


Fig. 7. Delay versus bias voltage characteristic of the voltage-controlled buffer measured at $V_{dd} = 5$ V, $T = 20°$C.

Four tapped buffer lines working as two identical VDL's were laid-out in straight lines to prevent unavoidable delay mismatch caused by folding the delay line into two or more sections [4]. The replica VDL, used in the DLL, is an exact layout copy of the VDL used for measurements. In order to make sure that all capacitances that may influence the buffer delay are as well matched as possible, the replica includes also a copy of circuits loading the delay buffers. The arbiter circuit was constructed as a cross-coupled pair of NAND gates, as in Fig. 8. The first rising edge at one of the inputs, A or B, causes the corresponding output to go low, which in turn latches the other output high. A simple finite-state machine controls the DLL. Using a reference clock, it produces the necessary input signals for the VDL, waits until they have finished propagating in the delay line, and then sets the direction of the charge pump according to the state of the arbiter, thus enabling the appropriate correction of $V_{\rm BIAS}$. The charge pump current can be adjusted externally in a range of 0–100 μA to ensure that the amplitude of $V_{\rm BIAS}$ corrections can be controlled. The filter capacitor C_F is implemented as a large pMOS gate capacitance surrounded by guard rings to minimize the noise coupling through the substrate. The value of this capacitor is approximately 0.3 nF.

To enable comprehensive characterizations of the delay lines, the DLL locking mechanism may be disabled. With the DLL enabled, the resolution is determined by the reference clock frequency according to (3). For the resolution of 60 ps, the clock frequency is equal to 130.208 MHz. Other resolutions may be obtained by varying the clock frequency in a range of 30–265 MHz. With the DLL disabled, the TDC resolution may be set in a range of 0–300 ps, by externally setting $V_{\rm BIAS}$ to a fixed value. For test purposes, a number of internal signals have been connected to the test pins.

The read-out circuitry uses a parallel-input/serial-output register. The state of the VDL can be latched into this 128-bit register, and then the result of the conversion can be shifted out through the serial-output port. This configuration reduces the functionality of the TDC as compared with the asynchronous read-out architecture described above; however, it enables a comprehensive characterization of the VDL performance.

IV. Experimental Results

Integrated circuits were fabricated through EUROPRACTICE. Out of ten chips, eight were fully functional. The chips were tested in a laboratory environment based on the GPIB (IEEE-488) interface bus, which allowed the automatic repetition of large number of measurements necessary for statistical analysis of errors. A DG535 timing generator was used to generate an input time interval between START and STOP pulses. This instrument has a 5-ps resolution and a specified maximum 25-ps time jitter, although measurements indicate that it was somewhat smaller.

TABLE I
Transistor Dimensions

Transistor	type	W [µm]	L [µm]
voltage-controlled buffer			
M1	p	28	1.2
M2	n	28	1.2
M3	n	28	1.2
M4	n	12	3.0
non-controlled buffer			
M1	p	28	1.4
M2	n	28	1.4

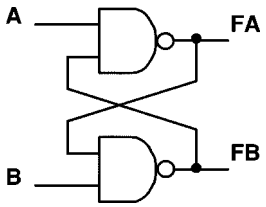


Fig. 8. Arbiter circuit.

A. TDC Characteristics

Referring to (1), the TDC measures the input time interval t_X. Since the VDL is 128 stages long, the conversion result read-out from the chip n_X can be represented as a 7-bit number, with the 1 LSB equivalent to the time resolution t_R. The conversion characteristic (i.e., n_X as a function of t_X) with t_R set to 150 ps is presented in Fig. 9(a). It was obtained by performing consecutive measurements while sweeping t_X value from 0 to 20 ns in 5-ps intervals. (In practice, the value n_X is affected by a constant offset between START and STOP pulses, caused by mismatched wires and by setup times of the latches in the delay line, which must be subtracted from every measurement. All of the figures show characteristics after this offset calibration.) The maximum integral nonlinearity of the characteristic is less than $\pm$1/2 LSB, while the root mean square (RMS) value, calculated as

$$\mathrm{INL_{RMS}} = \frac{1}{t_{\rm DR}}\sqrt{\int_0^{t_{\rm DR}} (t_X - n_X t_R)^2\, dt_X} \qquad (5)$$

is equal to 46 ps. This includes a $t_R/\sqrt{12}$ quantization error of 43.2 ps, and therefore, the nonlinearity error alone is equal to 16 ps RMS.

B. Resolution Set by the DLL

With the DLL loop enabled, the voltage $V_{\rm BIAS}$ is set automatically in the feedback loop to maintain $t_R = T_{\rm clk}/N$ constant (2), despite ambient condition changes. The values of $V_{\rm BIAS}$ set

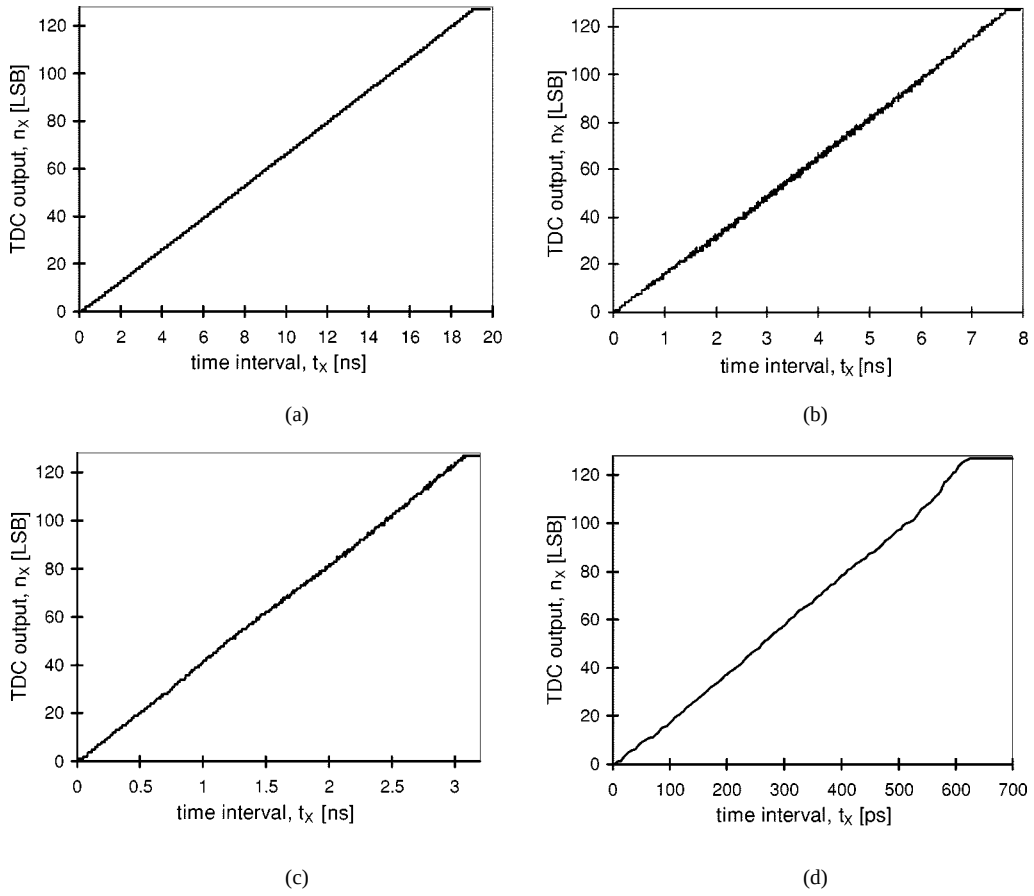


Fig. 9. TDC conversion characteristics: (a) DLL disabled, $t_R = 150$ ps, single shot, (b) DLL enabled, $t_R = 60$ ps, single shot, (c) DLL disabled, $t_R = 25$ ps, single shot, and (d) DLL disabled, $t_R = 5$ ps, averaged over 50 measurements.

in the DLL against the reference clock frequency $T_{\rm clk}$, for various temperature and power supply values are plotted in Fig. 10. The DLL loop functions for $T_{\rm clk}$ clock frequencies up to 265 MHz, which corresponds to a resolution of less than 30 ps.

When the DLL loop is enabled, a random noise appears on the TDC characteristics. Results of one-shot measurements, at 60-ps resolution, are presented in Fig. 9(b). The input pulse time was swept from 0 to 8 ns with a 5-ps step. The TDC output includes 45-ps RMS random error. This error is caused by random time jitter and therefore may be suppressed by averaging results over many measurements. The average characteristic shows a total RMS nonlinearity of 20 ps, with the maximum integral nonlinearity better than ± 1 LSB. Indeed, in typical spectrometry applications, the final result is obtained by statistical analysis of the results of many measurements, and therefore, random error will be averaged.

It also has to be noted that the mismatch between the VDL used for measurements and the replica VDL working in the DLL may cause a systematic gain error of the characteristics. This error is mostly due to the random variations of circuit parameters and will therefore vary from chip to chip. For various chips (eight were tested), the gain error was from −2% to 1%, with some chips exhibiting virtually no gain error.

For higher resolutions, as the clock frequency is increased, the measured time jitter also increases, with total RMS error reaching the maximum value of 58 ps for DLL working at 30 ps resolution. This illustrates that the layout of the circuit has to be designed very carefully to minimize the effect of switching digital signals on delay values. This relatively large jitter error appears only when the DLL is in operation. Therefore, one simple way to increase the accuracy is to disable the DLL during measurements and allow it to set the value of $V_{\rm BIAS}$ in between the measurements. This presents no problem as the large capacitance of C_F holds the value of $V_{\rm BIAS}$ virtually constant for as long as a few seconds. By this means, it is estimated that resolutions of up to 30 ps with accuracy better than ± 1 LSB can be achieved. Fig. 11(a) shows the measured single-shot nonlin-

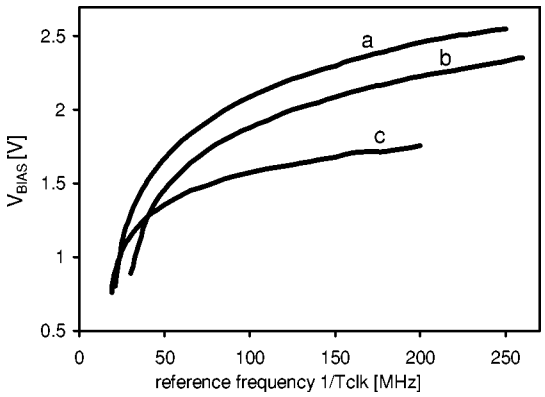


Fig. 10. Voltage $V_{\rm BIAS}$ set in the DLL loop for various power supply voltages and ambient temperatures as a function of reference frequency: (a) $V_{DD} = 5$ V, $T = 80°$C, (b) $V_{DD} = 5$ V, $T = 20°$C, and (c) $V_{DD} = 3.3$ V, $T = 20°$C.

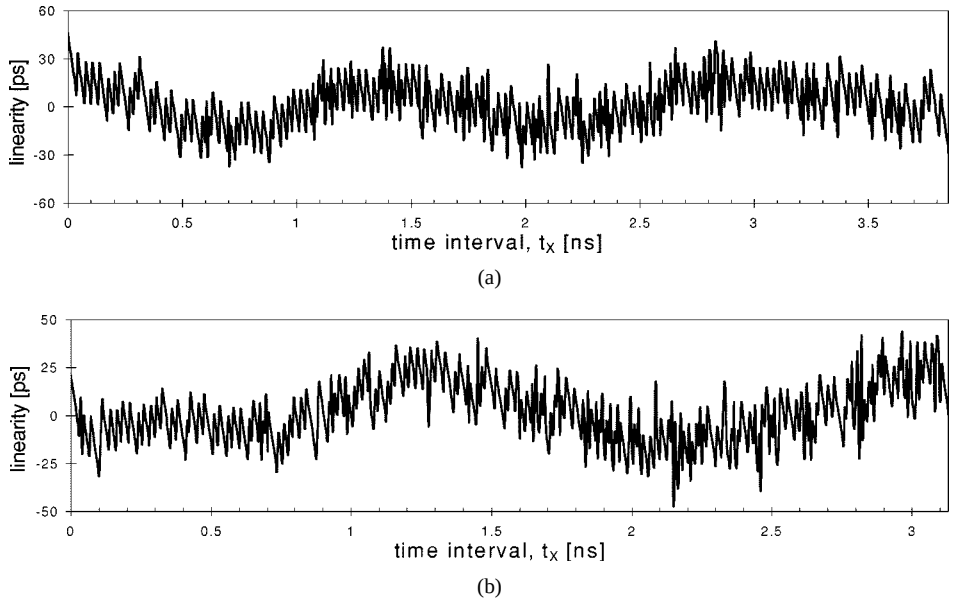


Fig. 11. TDC nonlinearity characteristics: (a) DLL disabled, $t_R = 30$ ps, chip 2 and (b) DLL disabled, $t_R = 25$ ps, chip 3.

earity error of the characteristic for the resolution of 30 ps, with the DLL turned off.

C. Higher Resolutions

Further measurements were conducted with the chip working at even higher resolutions, with external biasing. The DLL is disabled, and V_{BIAS} is forced to the appropriate value. Fig. 9(c) shows the single-shot characteristic for resolution of 25 ps, and Fig. 11(b) shows the nonlinearity of this characteristic. Overall RMS error of the characteristic is equal to 16 ps, whereas the maximum integral nonlinearity is equal to approximately ±30 ps. For higher resolutions, the nonlinearity error becomes more significant. However, it also has to be noted that the systematic integral nonlinearity errors could be suppressed by a numerical linearization of the TDC characteristics. This can be performed by a host computer that can adjust the result read-out from the TDC using a lookup table containing the nonlinearity error characteristic, obtained during a calibration procedure.

The nonlinearity of the characteristics is caused by the random mismatch of the buffer delays and by the crosstalk between START and STOP pulses. This last cause seems to be the dominant one, since for various chips, we have obtained similar nonlinearity characteristics. Also, for different resolutions, the nonlinearity characteristics are correlated in time much stronger than according to the position in the delay line. This can be seen, comparing the characteristics of Fig. 11, as plotted for various chips and resolutions. The input pulses were carefully screened on the test printed circuit board, however, insufficient attention was paid to reduce the crosstalk on chip (in particular, START and STOP test pads were unfortunately located next to each other).

With external biasing, much higher resolutions are possible, however there will be a limit where due to variations of buffer delays, the VDL goes nonmonotonic, i.e., single STOP pulse will be registered as a number of HI/LO transitions in the output word. For our chip, this limit is around 5 ps. Also, for such high resolutions, random jitter will be a significant error factor for single-shot measurements. Nevertheless, the average characteristic of the chip working with a 5-ps resolution obtained by averaging the results of 50 measurements, which is plotted as Fig. 9(a), shows surprisingly good linearity. This is attributed to the fact that as can be inferred from Fig. 11, the crosstalk between START and STOP signals does not much affect the linearity for the maximum measured time of less than 500 ps. Also, the time-jitter noise, both generated in the delay line and coming from the pulse generator used, actually improves (smooths) the average characteristics, so the differential nonlinearity error in the 5-ps resolution case might be actually larger than it is possible to measure with current experimental setup.

D. Time Jitter

To characterize time jitter in the delay lines, we observed the output of the TDC for a large number of measurements with fixed values of input time intervals t_X. Fig. 12(a) and (b) shows histograms of output values for 200 measurements with t_X equal to 190 ps and 11 ns. These correspond to the output values generated, respectively, near the beginning and end of the VDL working with the $t_R = 10$ ps. As could be expected for each measured time interval, the output values spread across several positions approximating the Gaussian error distribution. Moreover, the jitter is larger for larger values of t_X. If we assume that a single stage introduces time-jitter error of σ_{jitter} (RMS value) and that jitter values in different stages are uncorrelated, we obtain the RMS value of the error at the nth position in the line σ_n equal to

$$\sigma_n = \sqrt{\sum_{i=1}^{n} \sigma_{\mathrm{jitter}}^2} = \sqrt{n} \cdot \sigma_{\mathrm{jitter}}. \tag{6}$$

The measurement results show time jitter of 5.9 and 9.1 ps at outputs median values equal to 19 and 111, respectively. Hence, the jitter error per stage, with DLL turned off, can be calculated from (6) as 0.7 ps. It has to be remembered that the maximum

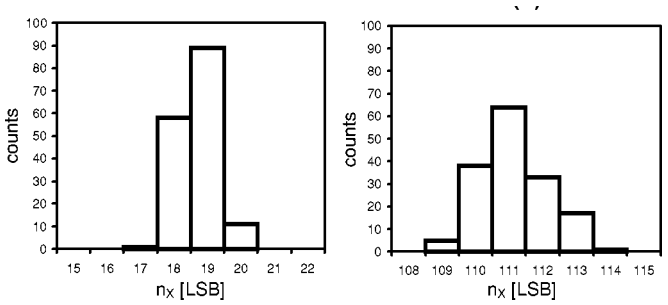


Fig. 12. Time-jitter measurements at the beginning and at the end of the delay line. Output value histograms for 200 consecutive measurements for $t_R = 10$ ps: (a) $t_X = 190$ ps and (b) $t_X = 11$ ns.

TABLE II
CHIP STATISTICS AND PERFORMANCE

Power supply voltage	5V
Die area	10mm^2
Process	0.7μm CMOS
No of transistors	11600
Length of the delay line	128
DLL locking resolutions	30ps to 250ps
Maximum integral non-linearity For t_R = 30ps	±30ps
Total single-shot error, rms For t_R=60ps, DLL on	45ps
For t_R=30ps, DLL off	20ps
Maximum time-jitter, rms DLL off	10ps
Maximum TDC resolution DLL off	~5 ps

jitter will occur at the end of the delay line. Moreover, some of the jitter can be generated in the input stages of the TDC. From our experiments, it can be concluded that the maximum value of time jitter in the delay lines, with the DLL turned off, is no greater than 10 ps RMS. (The results of these experiments also include unknown value of the time jitter caused by the pulse generator, though it can be seen that it must be less than 6 ps RMS.) With the digital circuitry of the DLL enabled and working at 125 MHz, measured jitter in the delay lines increases to around 5 ps per stage, reaching the value of 60 ps at the end of the delay line.

The chip performance and the measurement results are summarized in Table II.

V. CONCLUSION

A TDC chip utilizing VDL's has been presented. The experimental results confirm the ability of achieving very high temporal resolution using an integrated circuit fabricated in a standard digital CMOS process. A DLL can be used to stabilize the delay values against process variations and ambient conditions, although great care must be taken to avoid the increased error caused by signal coupling. The integrated circuit described here works with overall accuracy better than ±1 LSB for resolutions down to 60 ps, stabilized in the continuously working DLL loop or for resolutions down to 30 ps when the DLL loop is used intermittently to stabilize the delay between measurements, or in averaging mode. Alternatively, with external biasing, the VDL can achieve resolutions as high as 5 ps, however, the accuracy will be limited by the systematic nonlinearity error (which could be compensated using a lookup table) and by the random error of less than 10 ps RMS caused by the time jitter. By averaging this random error over several measurements, the accuracy may be further increased. We have also indicated how VDL's can be used in TDC systems with large dynamic range and low dead-time.

REFERENCES

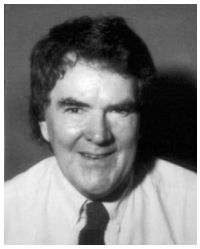
[1] M. A. Gruntman, "MASTIF: Mass analysis of secondaries by time-of-flight technique. A new approach to secondary ion mass spectrometry," *Rev. Sci. Instrum.*, vol. 60, no. 10, pp. 3188–3193, Oct. 1989.
[2] O. Saaski, T. Taniguchi, T. K. Ohsaka, H. Mori, T. Nonaka, K. Kaminishi, A. Tsukuda, H. Nishimura, M. Takeda, and Y. Kawakami, "1.2 GHz GaAs shift register IC for dead-time-less TDC application," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 512–516, Feb. 1989.
[3] A. E. Stevens, R. P. Van Berg, J. Van der Spiegel, and H. H. Wllliams, "A time-to-voltage converter and analog memory for colliding beam detectors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1748–1752, Dec. 1989.
[4] T. Rahkonen and J. Kostamovaara, "The use of stabilized CMOS delay line for the digitization of short time intervals," *IEEE J. Solid-State Circuits*, vol. 28, pp. 887–894, Aug. 1993.
[5] C. Ljuslin, J. Christiansen, A. Marchioro, and O. Klingsheim, "An integrated 16-channel CMOS time to digital converter," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 104–108, Aug. 1994.
[6] J. Christiansen, "An integrated CMOS 0.15 ns digital timing generator for TDC's and clock distribution systems," *IEEE Trans. Nucl. Sci.*, vol. 42, pp. 753–757, Aug. 1995.
[7] C. T. Gray, W. Liu, W. A. M. Van Niije, T. A. Hughes Jr., and R. K. Cavin III, "A sampling technique and its CMOS implementation with 1Gb/s bandwidth and 25 ps resolution," *IEEE J. Solid-State Circuits*, vol. 29, pp. 340–349, Mar. 1994.
[8] J. V. Hatfield, P. J. Hicks, and J. Goldfinch, "A 'when and where' charged-particle sensing system," *Sens. Actuators*, vol. A61, pp. 356–360, 1997.
[9] M. S. Gobrics, J. Kelly, K. M. Roberts, and R. L. Summer, "A high resolution multihit time to digital converter integrated circuit," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 379–384, June 1997.
[10] M. Johnson and E. L. Hudson, "A variable delay line PLL for CPU-coprocessor synchronization," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1218–1223, Oct. 1988.
[11] P. Dudek and J. V. Hatfield, "A zero dead-time, high temporal resolution, time-of-flight particle detector IC," in *Proc. Eurosensors XI Conf.*, Warsaw, Poland, Sept. 1997, pp. 1341–1344.
[12] M. J. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1439, Oct. 1989.

Piotr Dudek (S'00) received the five-year masters (mgr inż.) degree in electronic engineering from the Technical University of Gdańsk, Gdańsk, Poland, in 1997, and the M.Sc. degree from the University of Manchester Institute of Science and Technology (UMIST), Manchester, U.K., in 1996. He is currently working toward the Ph.D. degree at the same institution.

His research interests are in the area of analog and mixed-mode VLSI circuits, smart sensors, and massively parallel processor arrays.

Stanisław Szczepański received the M.S. and Ph.D. (with honors) degrees in electronic engineering from the Technical University of Gdańsk, Gdańsk, Poland, in 1975 and 1986, respectively.

In 1986, he was a Visiting Research Associate with the Institute National Polytechnique de Toulouse (INPT), Toulouse, France. From 1990 to 1991, he was with the Department of Electrical Engineering at Portland State University, Portland, OR, on a Kosciuszko Foundation Fellowship. From August to September 1998, he was a Visiting Professor with the Faculty of Engineering and Information Sciences at the University of Hertfordshire, Hatfield, U.K. He is currently an Assistant Professor and Head of the Department of Electronic Circuits, Faculty of Electronics, Telecommunications and Informatics, Technical University of Gdańsk. He has written approximately 60 publications and holds two patents. His teaching and research interests are in circuit theory, fully integrated analog filters, high frequency, low power analog integrated circuit design in bipolar and CMOS technology, and current-mode analog signal processing.



John V. Hatfield received the B.Sc degree in physics from the University of Leeds, Leeds, U.K., in 1973 and the M.Sc. degree from the University of Manchester Institute of Science and Technology (UMIST), Manchester, U.K., in 1984. He received thePh.D. degree by the same university in 1988 for his research in position-sensitive particle detectors.

Currently, he is a Reader in the Department of Electrical Engineering and Electronics at UMIST. His research interests are in the field of integrated sensors and transducers and he has published more than 70 papers in this area.