

THz operation of self-switching nano-diodes and nano-transistors

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ABSTRACT

By means of the microscopic transport description supplied by a semiclassical 2D Monte Carlo simulator, we provide an in depth explanation of the operation (based on electrostatic effects) of the nanoscale unipolar rectifying diode, so called self-switching diode (SSD), recently proposed in [A. M. Song, M. Missous, P. Omling, A. R. Peaker, L. Samuelson, and W. Seifert, Appl. Phys. Lett. 83, 1881 (2003)]. This device provides a rectifying behavior without the use of any doping junction or barrier structure (like in p - n or Schottky barrier diodes) and can be fabricated with a simple single-step lithographic process. The simple downscaling of this device and the use of materials providing high electron velocity (like high In content InGaAs channels) allows to envisage the fabrication of structures working in the THz range. With a slight modification of the geometry of the SSD, a lateral gate contact can be added, so that a nanometer self-switching transistor (SST) can be easily fabricated. We analyze the high frequency performance of the diodes and transistors and provide design considerations for the optimization of the downscaling process.

Keywords: ballistic transport, Monte Carlo simulation, terahertz devices, nanoscale rectifier

1. INTRODUCTION

A nanoscale unipolar rectifying diode based on electrostatic effects [so called self-switching diode (SSD)], was recently proposed in Ref. 1. This device provides an attractive rectifying I - V characteristic without the use of any doping junction or barrier structure. Moreover, its threshold voltage can be tuned from almost zero to more than ten volts by adjusting the channel width, W , and other geometric parameters. The simplicity of the technological process used for the fabrication of these diodes is also remarkable, since it only involves the etching of insulating trenches on a semiconductor surface (a single step of high resolution lithography). The downscaling of SSDs is so simple that, together with the intrinsically high electron velocity in some material systems, like those involving InGaAs channels, the fabrication of devices working in the THz range can be envisaged. Indeed, the high frequency performance of SSDs is dramatically improved thanks to a much shorter transit time, due not only to a smaller channel length but also to an enhanced electron velocity associated to ballistic transport. Moreover, a lateral gate contact can be added to the SSD (using also the trench-etching process) so that a nanometer self-switching transistor (SST) can be constructed with the same single technological step.

The basic operation of SSDs has been explained just in terms of the opening of the channel due to the accumulation of charges in the surrounding regions.¹ A detailed microscopic analysis of the behaviour of this device is essential to improve its performance. At this level, simulation tools constitute a valuable alternative to the expensive and time-consuming test-and-error procedure. Some theoretical descriptions of the operation of ballistic devices have been proposed²⁻⁴, always starting from a coherent transport description based on the Landauer-Buttiker formalism^{5,6}. In this work we will make use of a semiclassical 2D Monte Carlo (MC) simulation [successfully employed in previous works for the modelling of different types of InGaAs-based nanodevices: T- and Y-branch junctions and ballistic rectifiers⁷⁻¹¹] to explain the physics of the operation of InAlAs/InGaAs based SSDs and SSTs. MC simulations provide an insight of the processes taking place inside the devices, thus allowing us to relate the macroscopic results of the experiments with the microscopic behavior of electrons. Our model, based on a semiclassical transport description, is able to qualitatively reproduce the main features of the experimental results obtained in SSDs, thus demonstrating that, even if in some cases electrons move in quasiballistic fashion, coherent transport plays no significant role on the main characteristics of these devices.

We will mainly focus on the high frequency operation of SSDs and SSTs in order to define the geometry of the downscaled devices for achieving an optimized dynamic performance. In section 2 the MC model will be presented. Then, in Section 3, our model will be validated by comparison of the simulations with measurements performed in real SSDs, and some guidelines for the optimization of their performance will be given. In Section 4 SSTs will be studied and, finally, in Section 5 the main conclusions of this work will be drawn.

2. MONTE CARLO MODEL

We make use of a semiclassical ensemble MC simulator self-consistently coupled with a 2D Poisson solver. The transport model locally takes into account the effect of degeneracy and electron heating by using the rejection technique and the self-consistent calculation of the local electronic temperature and Fermi level¹². The surface charges appearing at the boundaries of the semiconductors in contact with dielectrics are also considered in the model¹³. The validity of this approach has been checked in previous works by means of the comparison with experimental results of static characteristics, small signal behavior and noise performance of a 0.1 μm gate AlInAs/InGaAs lattice matched HEMT.¹⁴ Since contact injection is a critical point when dealing with ballistic transport, the velocity distribution and time statistics of injected carriers will be accurately modeled following Ref. 15.

As seen in Fig. 1, where an AFM image of a fabricated SSD is shown, for the correct modeling of these devices, a 3D simulation would be necessary in order to take into account the effect of the lateral surface charges and the real geometry of the structures. However, if some simplifications and assumptions are made, correct results can be obtained (in a shorter time) with a simpler 2D MC model. Indeed, two different types of 2D simulations can be performed, front-view (FV) and top-view (TV). Within the FV simulations the layer structure is taken into account, but the device in the z dimension is considered to be homogeneous. This kind of simulations can be useful for the modeling of simple structures, like homogeneous channels or classical transistors^{7, 8, 12, 14}. On the other hand, to account for the top geometry of more complicated devices (such as our SSDs and SSTs) TV simulations will be carried out. They are performed in the xy plane; therefore the real layer structure is not included, and only the InGaAs channel will be simulated [see the sketch of Fig. 1(b)]. To account for the fixed positive charges of the whole layer structure, a net doping is assigned to the channel in TV simulations, but impurity scattering is switched off. In this way the electron transport through the undoped channel is well reproduced, since this is a “virtual” doping associated with the charges of the cap and δ -doped layers. On the other hand, a negative surface charge density is assigned to the semiconductor-air interfaces to account for the influence of the surface states originated by the etching processes. Therefore, to ensure the accuracy of this TV approximation the values of two important parameters must be carefully chosen: the background doping in the channel, N_{Db} , and the lateral surface charge density, σ .

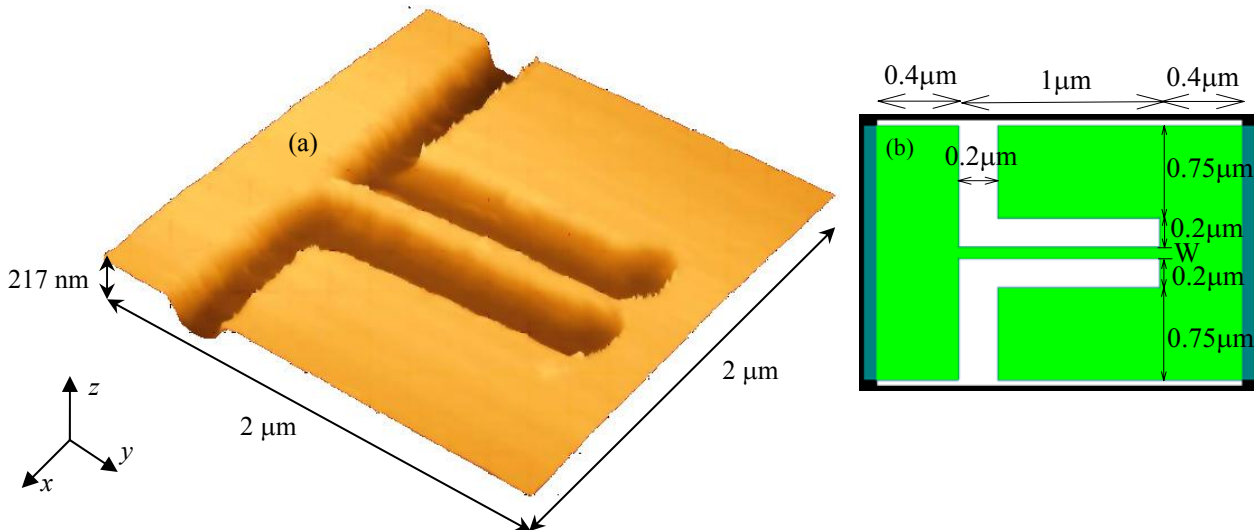


Figure 1: (a) AFM image of a fabricated SSD and (b) geometry of the top-view simulation domain (white regions represent a dielectric).

3 SELF SWITCHING DIODES

Fig. 2 shows the I - V curves measured in SSDs with different channel widths, W , compared with the results of the MC simulations of similar devices [the geometry of the fabricated SSDs is shown in the AFM picture of Fig. 1(a) and the simulation domain is sketched in Fig. 1(b)]. The good agreement obtained with the 2D top-view simulations (considering a background doping $N_{Db}=10^{17} \text{ cm}^{-3}$ and a surface charge density $\sigma=0.3 \times 10^{12} \text{ cm}^{-2}$) confirms the validity of our approximations.

Even if the real geometry of the measured devices is not precisely known, the main features of the experimental devices are well reproduced by the MC simulation; namely, the current rectification and the increase of the threshold voltage when the channel is narrowed. The non-simulated dimension Z used for the comparison with the experimental current was estimated by using the measured Hall sheet density $n_s=10^{12} \text{ cm}^{-2}$, giving a value for $Z=n_s/N_{Db}=10^{-5} \text{ cm}$. However, a precise knowledge of the geometry of the real devices would be necessary for the fine adjustment of the simulation (i.e., the determination of the surface charge to be considered in the simulations), since the current is strongly dependent on W and σ .

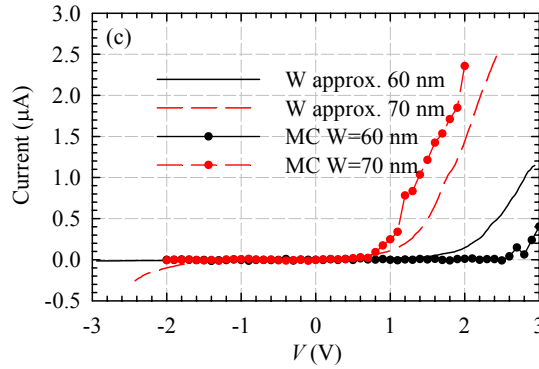


Figure 2: Comparison of the measured and simulated I - V characteristics of SSDs with different channel widths.

In order to have a better charge control in the channel we have simulated SSDs in which the width of the lateral trenches has been reduced to 60 nm. In this way the inverse leakage current is avoided even for wide channels, Fig. 3(b).

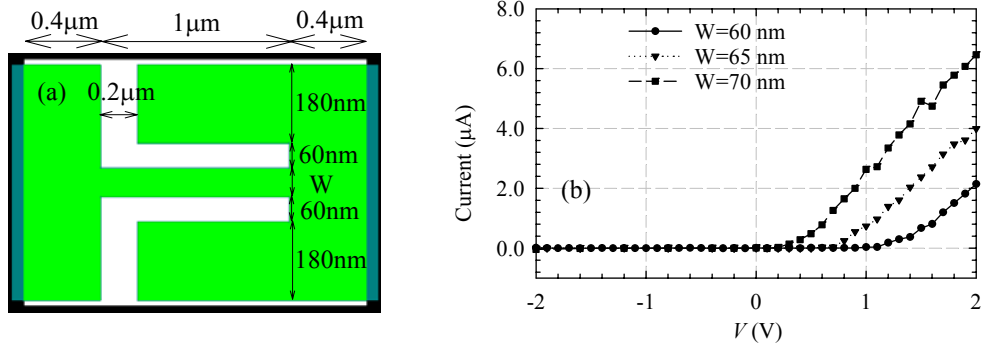


Figure 3: (a) Geometry of the simulated SSDs and (b) I - V curves of the devices with different W .

The basic operation of the SSD was roughly explained in (1) in terms of the opening of the channel due to the accumulation of charges in the regions surrounding the trenches that define the channel. We will exploit the microscopic description of transport given by the MC simulations to provide an in-depth explanation of the physics involved in the self-switching operation.

In Fig. 4 the electric potential inside the SSD of Fig. 3(a) with $W=70 \text{ nm}$ is plotted for $V=+2.0 \text{ V}$, 0.0 V and -2.0 V . It can be observed that the voltage applied to the anode (right contact) propagates to the vicinity of the channel. At

equilibrium the channel is closed due to the depletion induced by the surface charges located at the lateral walls. When $V > 0$, the positive potential reaches the lateral regions of the SSD channel, so that the potential barrier is lowered (or even removed, as observed for $V = 2.0$ V), thus allowing the electron flow (the channel is open). On the contrary, when $V < 0$ the potential profile in the right part of the device and in the channel is almost unchanged with respect to the equilibrium situation.

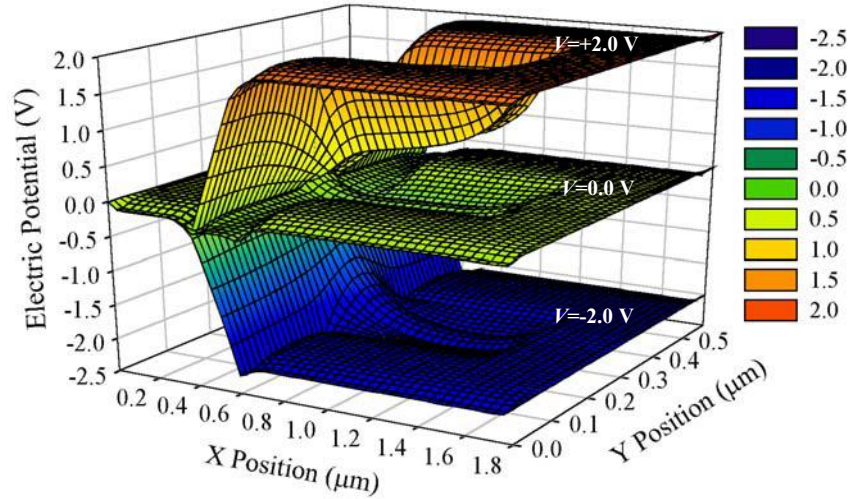


Figure 4: Electric potential inside the SSD of Fig. 3 with $W = 70$ nm for $V = -2.0$ V, 0.0 V and $+2.0$ V.

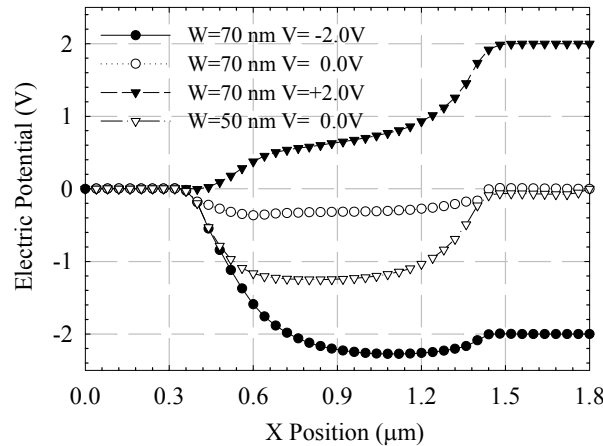


Figure 5: Profile of the electric potential along the channel of the SSD with $W = 70$ nm for $V = -2.0$ V, 0.0 V and $+2.0$ V. The equilibrium case for the SSD with $W = 50$ nm is also plotted.

This evolution can be better observed in Fig. 5, where the potential profile along the center of the channel is plotted for different applied voltages. For $V = 0.0$ V and $V = -2.0$ V, the potential barrier obstructing the electron flow is present, while for $V = 2.0$ V it has disappeared, thus allowing the increase of the current. As observed in Fig. 5 in the equilibrium case, the height of the barrier becomes larger when the channel is narrowed, so that the threshold voltage needed to switch on the conduction is higher, thus explaining the behavior of the I - V characteristics shown in Fig. 2. Therefore, the operation principle of this device is just the same as that of an enhanced mode field effect transistor (the narrow channel is pinched off in equilibrium), in which lateral gates (in this case short-circuited to the drain) control the current flow through the channel.

It is important to remark that the operating principle of SSDs, unlike other semiconductor nanodevices (TBJs, YBJs, ballistic rectifiers),⁷⁻⁹ is not based on ballistic transport or high mobility, and therefore SSDs could also be fabricated on

Si, thus taking advantage of the well established Si technology. However, when downscaling the size of SSDs fabricated on high mobility materials, the high frequency performance of the devices can be dramatically improved thanks to a much shorter transit time, due not only to the shorter channel length but also to the enhanced electron velocity associated with ballistic transport.

The I - V curves of SSDs with $W=50$ nm and different channel lengths (ranging from $L=1.0$ μm to $L=100$ nm) are shown in Fig. 6. In order to further optimize the current control of SSDs, we have reduced the width of the trenches to 5 nm (near the limits of up-to-date technology), so that the potential applied to the right contact affects more strongly the population of the channel. As observed in the figure, short channel effects (comparable to those found in traditional FET transistors) appear when the aspect ratio of the channel (L/W) decreases. In such a case, under inverse bias the potential of the lateral regions may not be able to deplete the channel, so that the barrier preventing the current flow disappears and an inverse leakage current flows (as observed for $L=100$ nm). This may happen because of a too wide channel or too wide lateral trenches. The very thin trenches of the devices analyzed in Fig. 6 not only prevent the presence of inverse leakage current for very short channels (it only appears for $L=100$ nm), but also the forward current is much improved. For high applied voltages a tendency to saturation associated with hot-carrier effects is observed in the current.

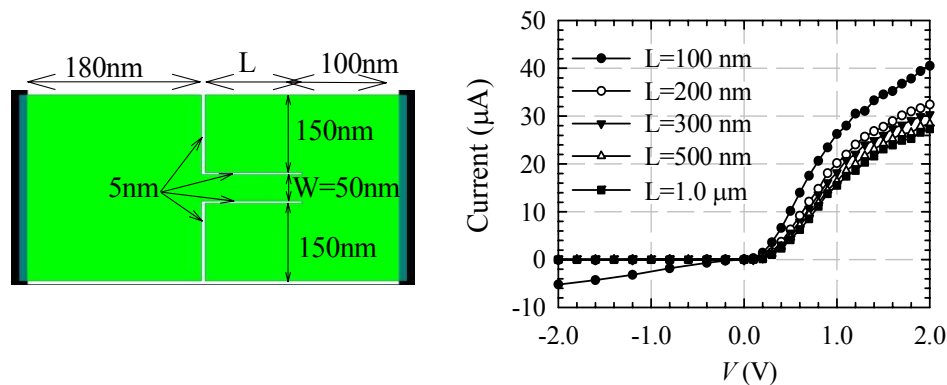


Figure 6: (a) Geometry of the simulated SSDs ($W=50$ nm, 5 nm wide trenches) and (b) I - V curves for different channel lengths L .

The dynamic behavior of these optimized devices can be tested by means of the MC simulation of their response to sinusoidal input voltage signals of increasing frequency. Fig. 7 shows the time-dependent current in the SSDs of Fig. 6 with $L=100$ nm and $L=300$ nm for input voltages with an amplitude of 0.5 V and different frequencies (100 GHz, 0.5 THz and 1 THz). The displacement current associated to the variation of the applied voltage is not considered here, since its average value is null and for high frequency it conceals the overall current response. For 100 GHz, the rectification is quite good (nearly following the static behavior), the shorter structure exhibiting a higher forward current even if a small inverse conduction is present, as expected from the static I - V characteristics. When increasing the frequency of the applied signal (0.5 and 1.0 THz), the shape of the current is degraded and a dephasing in the response appears, but it still shows a positive average value.

This is better observed in Fig. 8, where the mean value of the current is represented as a function of the frequency of the periodic input voltage. As expected, the cut-off frequency of the rectifying behavior of SSDs depends on the channel length, being lower for longer channels. The current overshoot observed in Fig. 7(c) leads to an increase of the DC response for input signal frequencies around 1 THz (Fig. 8). This overshoot comes from a kind of resonance originated, when transport is ballistic, by the coincidence between the transit time of electrons and the period of the applied signal. In fact, only for ballistic channels ($L<300$ nm) an increase of DC response is observed before its decay, while the diffusive ones show a normal cutoff (Fig. 8). The structure with $L=100$ nm is correctly responding up to frequencies over 2.0 THz, thus making possible the operation of these devices as, for example, power detectors of THz waves (or T-rays)¹⁶. However, we have to note that these intrinsic high-frequency capabilities are likely to be deteriorated by the extrinsic contact resistances and capacitances. Therefore, strong efforts (both at technologic and design levels) must be made to minimize their effect.

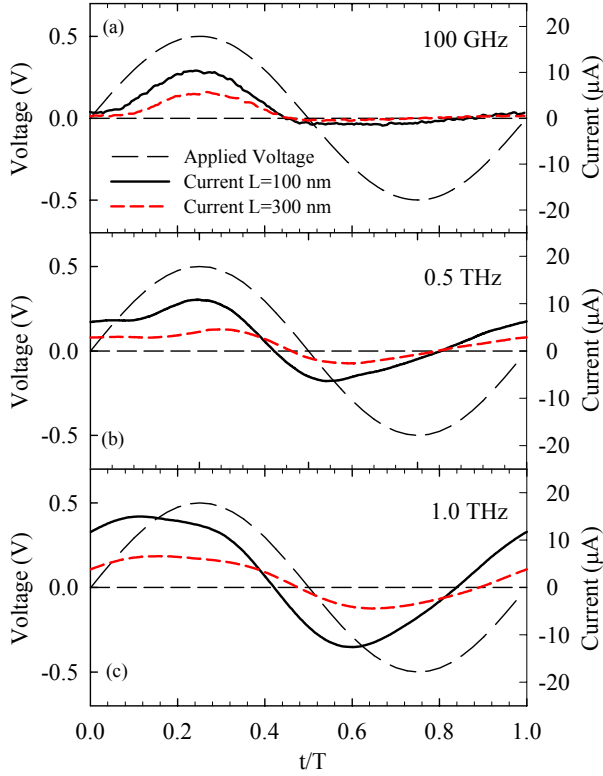


Figure 7: Current response to input voltages with amplitude of 0.5 V and frequencies of (a) 100 GHz, (b) 0.5 THz and (c) 1.0 THz applied to the SSDs of Fig. 6 ($W=50$ nm, 5 nm wide trenches) with channel lengths $L=100$ nm and $L=300$ nm.

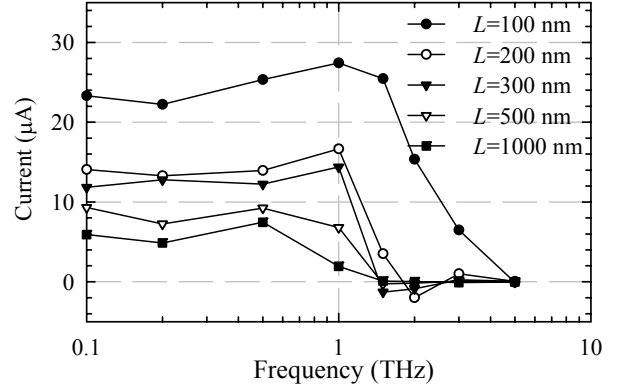


Figure 8: Mean current vs. frequency of the periodic voltage (with amplitude of 0.5 V) applied to the SSDs of Fig. 6.

Ballistic transport has also very interesting consequences on the behavior of the noise generated within SSDs. We have performed calculations of the current noise spectral density at low frequency, $S_I(0)$, of the SSDs. Full shot noise [$S_I(0)=2qI$, q being the electron charge and I the current] is expected to appear when the electron flow through the channel is completely ballistic and the carriers are uncorrelated. However, shot noise suppression can take place when transport is not ballistic [diffusion noise is lower than shot noise] or electrons are correlated (through Pauli Exclusion Principle or Coulomb interaction).¹⁵ In Fig. 9 the results of $S_I(0)$ in an SSD with $L=250$ nm, $W=50$ nm and 5 nm wide trenches are compared to $2qI$.

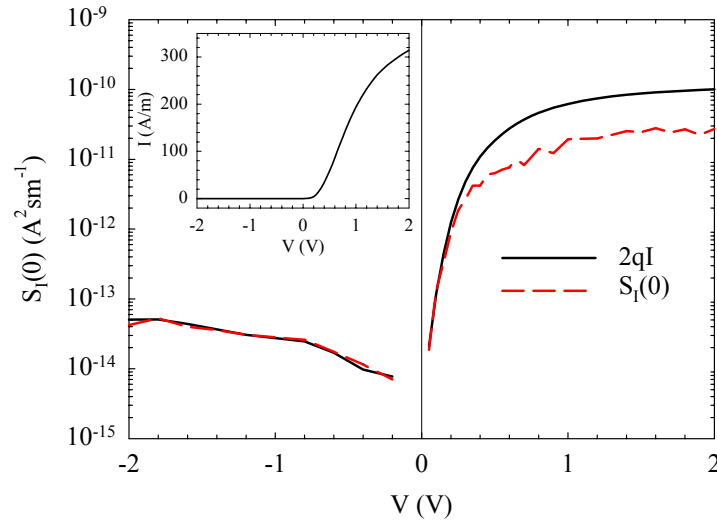


Figure 9: $S_I(0)$ and $2qI$ in an SSD with $L=250$ nm, $W=50$ nm and 5 nm wide trenches, whose I - V curve is shown in the inset.

The figure shows that full shot noise is found not only under inverse but also under direct bias below a certain threshold potential, above which the level of noise is lower than $2qI$. In order to explain this different behavior Fig. 10 shows the Fano Factor, $F=S_I(0)/2qI$, together with the value of the potential barrier for electrons flowing from anode to cathode and from cathode to anode (right and left directions, respectively). The barrier in the left direction is always large (even if it slightly decreases under inverse bias), while that in the right direction decreases and then vanishes when increasing the applied direct potential, thus providing the previously explained rectification. As long as the barrier has a significant value (higher than about 0.1 eV), and consequently the current is not high, the SSD displays full shot noise (both under direct and inverse bias) with $F=1$. When the direct bias is increased, the potential barrier for electrons flowing from cathode to anode is lowered, so that the channel resistance decreases. Under these conditions, the diffusive accesses to the channel become more and more important in the total noise of the device, $S_I(0)$ thus showing an increasingly suppressed value with respect to the full shot noise ($F<1$). When the barrier disappears, F reaches a constant value of about 0.3, just related to the total resistance of the device. This specific value depends on the geometry of the SSD. In contrast the appearance of full shot noise when the barrier is significant is independent of the device design as long as transport is ballistic.

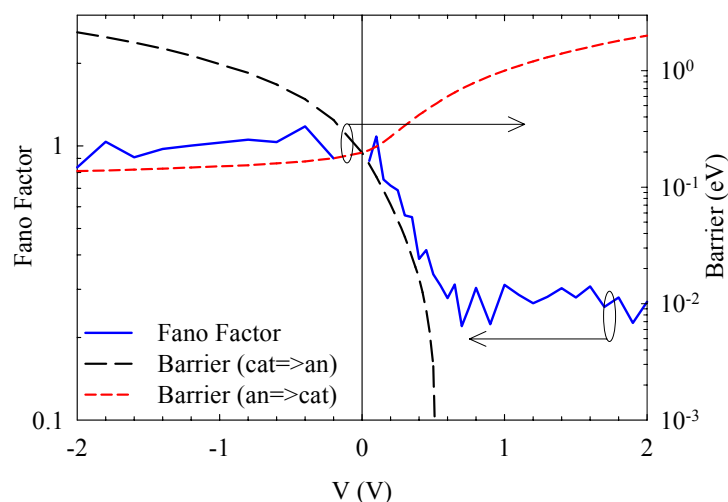


Figure 10: Fano factor and value of the potential barrier for electrons flowing from cathode to anode (right direction) and from anode to cathode (left direction) as a function of the potential applied to the anode.

3 SELF SWITCHING TRANSISTORS

With a small modification of the geometry of SSDs, as shown in Fig. 11(a), a control terminal (lateral gate) can be implemented in the device, thus becoming an SST. This third terminal, which acts as the gate of a typical FET transistor, controls the current flow through the channel, thus leading to the output characteristics shown in Fig. 11(b). The comparison with the I - V curve of the SSD with the same geometry (200 nm channel) indicates that the addition of the gate terminal degrades the rectification ability of the device (lower current under direct bias and higher inverse leakage). This happens because the drain bias, which provides the rectification in the SSDs, controls less efficiently the potential barrier inside the channel of the SST, which now is mainly fixed by the gate bias.

In order to maintain the self-switching behavior in the SSTs, the channel control must be shared by gate and drain by means of the potential applied to the top and bottom interfaces of the channel, respectively. In the device of Fig. 11 the prevalent effect comes from the gate potential. To reduce the influence of this contact and thus balance gate and drain effects, a wider trench between gate and channel will be considered [Fig. 12(a)]. Figs. 12(b) and (c) show how the current rectification is improved as the trench width, d , is enlarged. However, this modification has the drawback that the gate control of the drain current is lower, and consequently the transconductance, g_m , of the SST decreases. Indeed, for $V_{ds}=1.0$ V and $V_{gs}=0.0$ V, g_m goes from around 20 μ S for the SST with $d=5$ nm (that of Fig. 11) to around 10 μ S for $d=20$ nm and around 7 μ S for $d=30$ nm (those of Fig. 12).

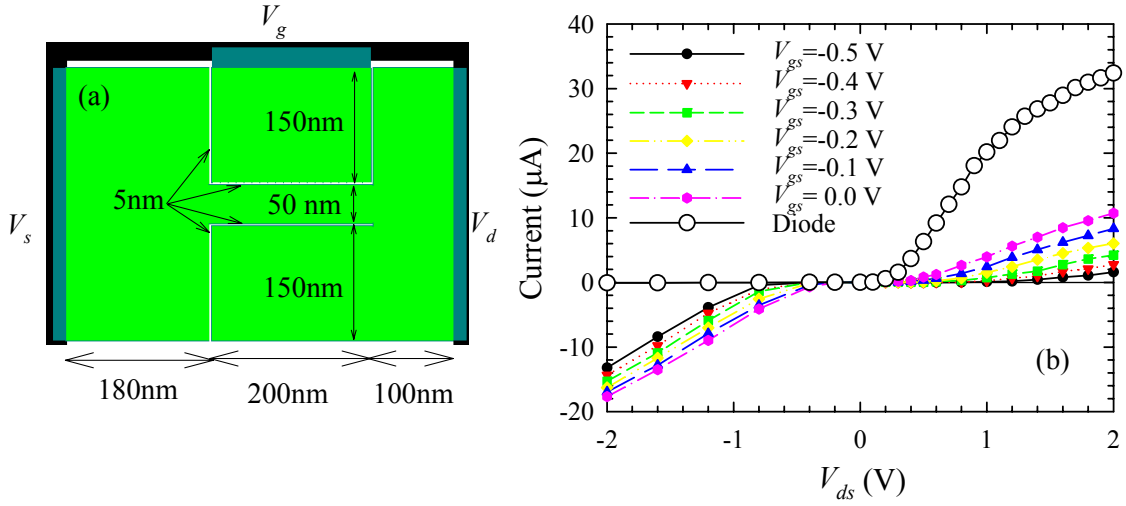


Figure 11: (a) Geometry of the simulated SST ($L=50$ nm, $W=50$ nm, 5 nm wide trenches) and (b) output characteristics together with the I - V curve of the SSD with the same geometry.

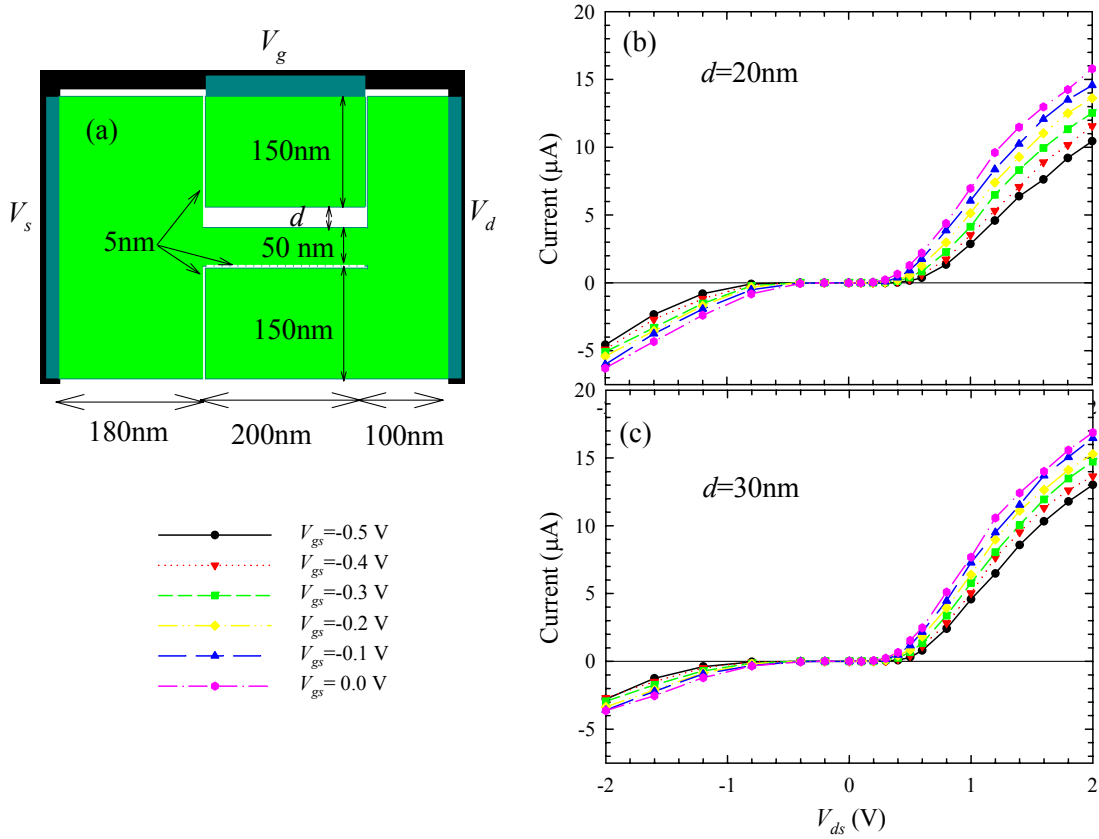


Figure 12: (a) Geometry of SSTs with a larger separation between gate and channel, d , and output characteristics of the SSTs with (b) $d=20$ nm and (c) $d=30$ nm.

4 CONCLUSIONS

By means of a semiclassical MC simulation we have explained the physics of the rectifying behavior of SSDs, based on the propagation of the voltage applied to the anode to the vicinity of the channel, thus controlling the current flowing

through it (just like a classical FET device). The optimization of the SSD performance can be achieved by reducing the channel length and the thickness of the trenches used to define the geometry. We have also shown that, if correctly designed, the intrinsic cutoff frequency of an optimized device can reach the THz range, so that SSDs could be used as T-ray detectors. Full shot noise has been observed in SSDs while the ballistic channel is the most resistive region of the device (a significant potential barrier is present and the current is not high), while a constant shot noise suppression (dependent on the SSD geometry) is found above a certain direct bias for which the barrier vanishes. Finally we have demonstrated the operation of SSTs, in which the rectification is degraded as compared to the SSDs. In order to maintain the asymmetric characteristics the gate electrode must be somewhat separated from the channel.

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